SNS COLLEGE OF TECHNOLOGY

An Autonomous Institution Coimbatore-35

Department of Artificial Intelligence and Data Science

23EET103 Electric Circuits and Electron Devices

I B.TECH-CSE-IOT/ II SEMESTER

UNIT IV : ELECTRONIC DEVICES AND APPLICATIONS

Topic : - Working principle and characteristics of JFET

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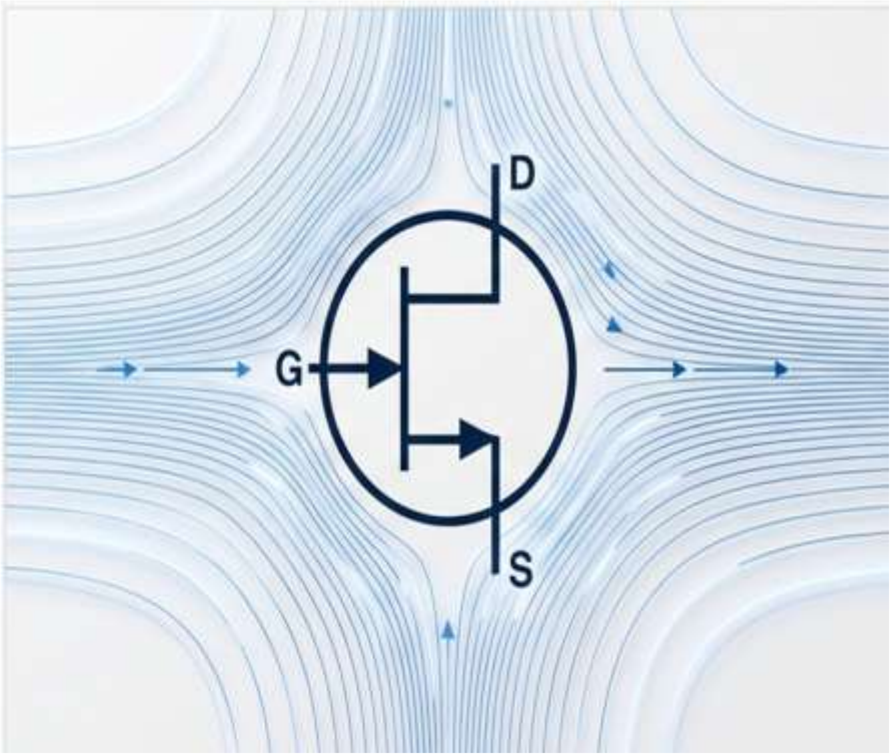
ASP/AIDS

Let’s Recall!!

- **Semiconductor basics** – n-type and p-type materials and charge carriers (electrons and holes).
- **PN junction diode** – depletion region, forward bias and reverse bias operation.
- **Current flow in semiconductors** – movement of electrons and holes under applied voltage.
- **BJT**-Working Principle and Types.

Topics for discussion

- Introduction to JFET (Junction Field Effect Transistor)
- Construction and Structure of JFET
- Types of JFET – N-Channel and P-Channel
- Working Principle of JFET
- Pinch-Off Voltage and Channel Control
- Regions of Operation (Ohmic, Saturation, Cutoff)
- Drain Characteristics of JFET
- Transfer Characteristics of JFET
- Advantages of JFET (High Input Impedance, Low Noise)
- Applications of JFET (Amplifiers, Switches, Buffer Circuits)



Why to Study JFET? *DT-Empathize*

The Problem: BJT Limitations

Standard Bipolar Junction Transistors (BJTs) are current-controlled.

- Low Input Impedance
- Signal Loading Effect
- Base Current Requirement

Draws current from the source, distorting delicate signals like human heartbeats.

The Solution: JFET

Voltage-Controlled operation driven entirely by an electric field.

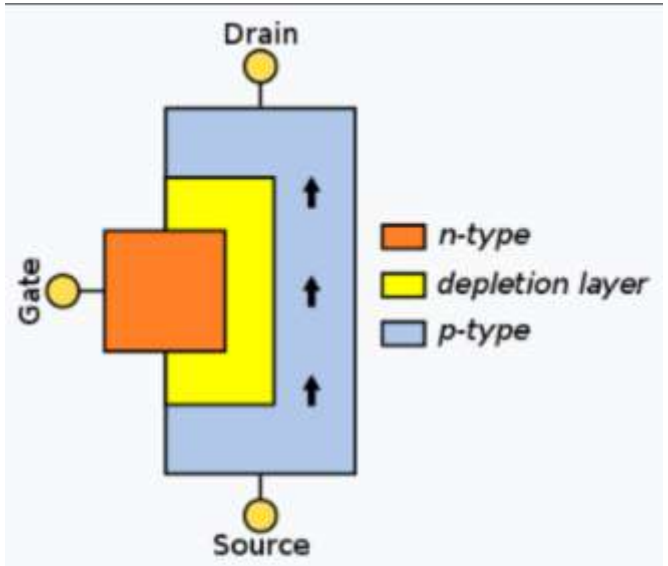
- Infinite Input Impedance (Typically > 10^9 Ω)
- Zero Gate Current
- Preserves Weak Signals

The gate junction is reverse-biased, ensuring minimal loading on driving circuits.

What is JFET

DT-DEFINE

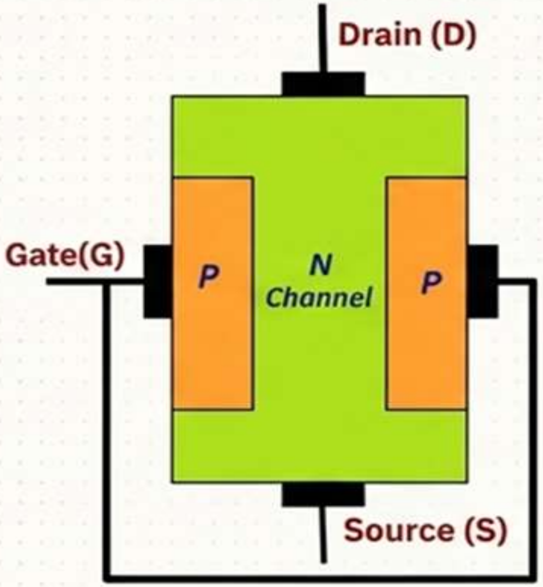
- JFET is a **three-terminal semiconductor** device consisting of Gate, Source, and Drain.
- It is a **voltage-controlled device**, where the gate voltage controls the current flow in the channel.
- JFET is a **unipolar device**, meaning current conduction occurs due to only one type of charge carrier (electrons or holes).
- It controls current through a semiconductor channel using an electric field.
- The gate is reverse biased, resulting in very high input impedance and nearly zero gate current.



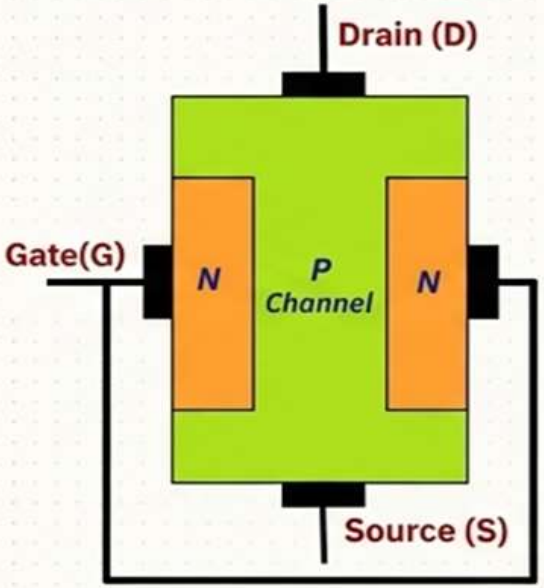
Terminal	Symbol	Role
Gate	G	Controls current flow via electric field
Source	S	Entry point of charge carriers
Drain	D	Exit point of charge carriers

Types of JFET

Source (S): Entry point of charge carriers.	**Drain (D):** Exit point of charge carriers.	**Gate (G):** Heavily doped PN junction controlling the channel.



Structure of N-Channel JFET



Structure of P-Channel JFET

N-Channel JFET

- Channel is N-type semiconductor
- Majority carriers: Electrons
- Controlled by a negative gate voltage
- Higher mobility, highly efficient

P-Channel JFET

- Channel is P-type semiconductor
- Majority carriers: Holes
- Controlled by a positive gate voltage

Working of JFET

- **Step 1 — No Bias (V_{GS} = 0)**

  When $V_{GS} = 0$ and a small V_{DS} is applied, maximum drain current (I_{DSS}) flows from Drain to Source. The depletion region is very small, allowing full channel conduction.

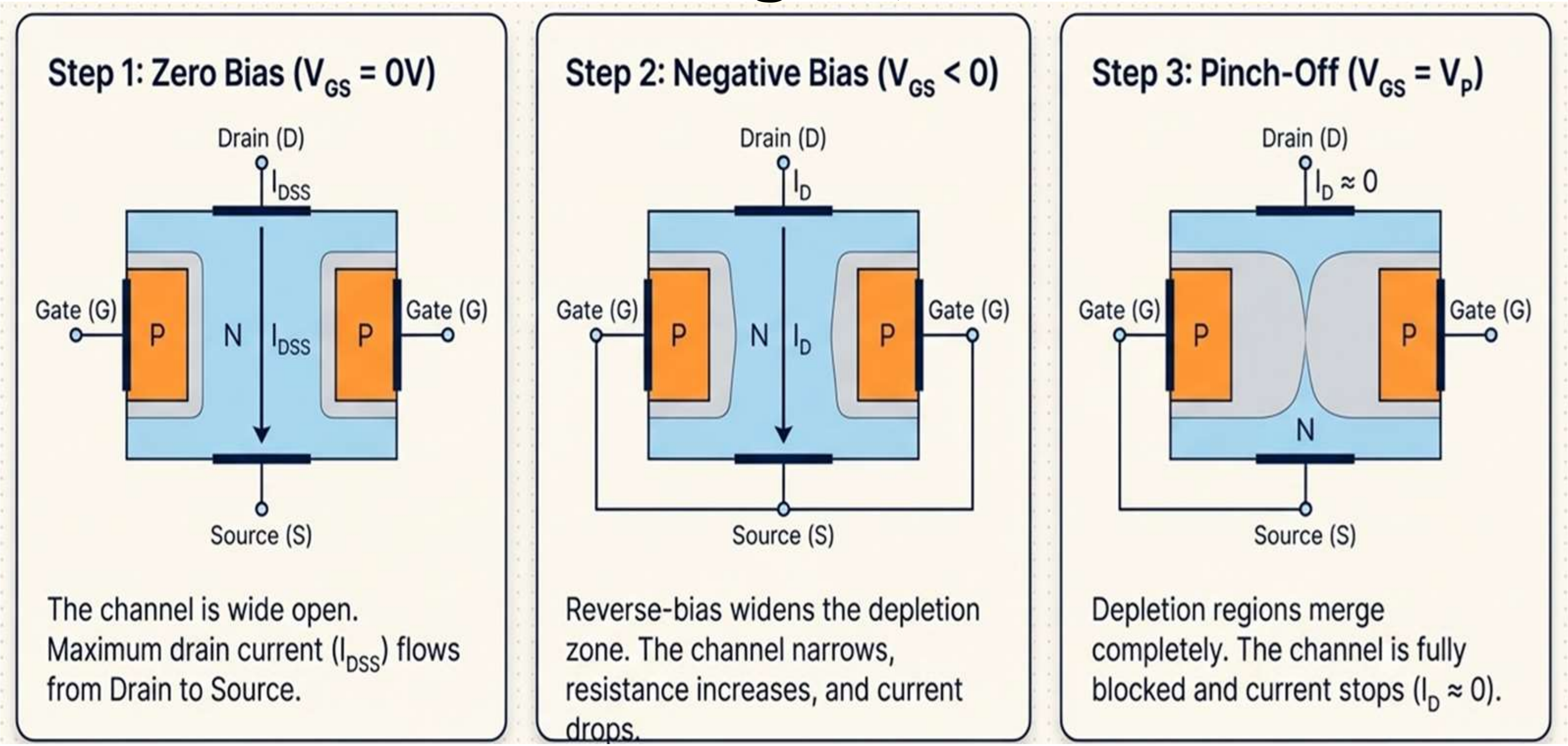
- **Step 2 — Negative Gate Voltage Applied ($V_{GS} < 0$)**

  A negative voltage at the Gate reverse-biases the PN junction, causing the depletion region to widen. This "squeezes" the channel, increasing its resistance and reducing drain current (I_D).

- **Step 3 — Pinch-Off ($V_{GS} = V_P$)**

  When V_{GS} reaches the Pinch-Off Voltage (V_P), the depletion regions meet at the center of the channel — the channel is completely blocked and $I_D \to 0$. This is the Cut-off region.

Working of JFET



Regions of Operation

Ohmic (Linear) Region

- **Condition:** $V_{GS} = 0$ (or low), low V_{DS}
- **Behavior:** Device acts as a voltage-controlled resistor. Current rises linearly with voltage.

Saturation (Active) Region

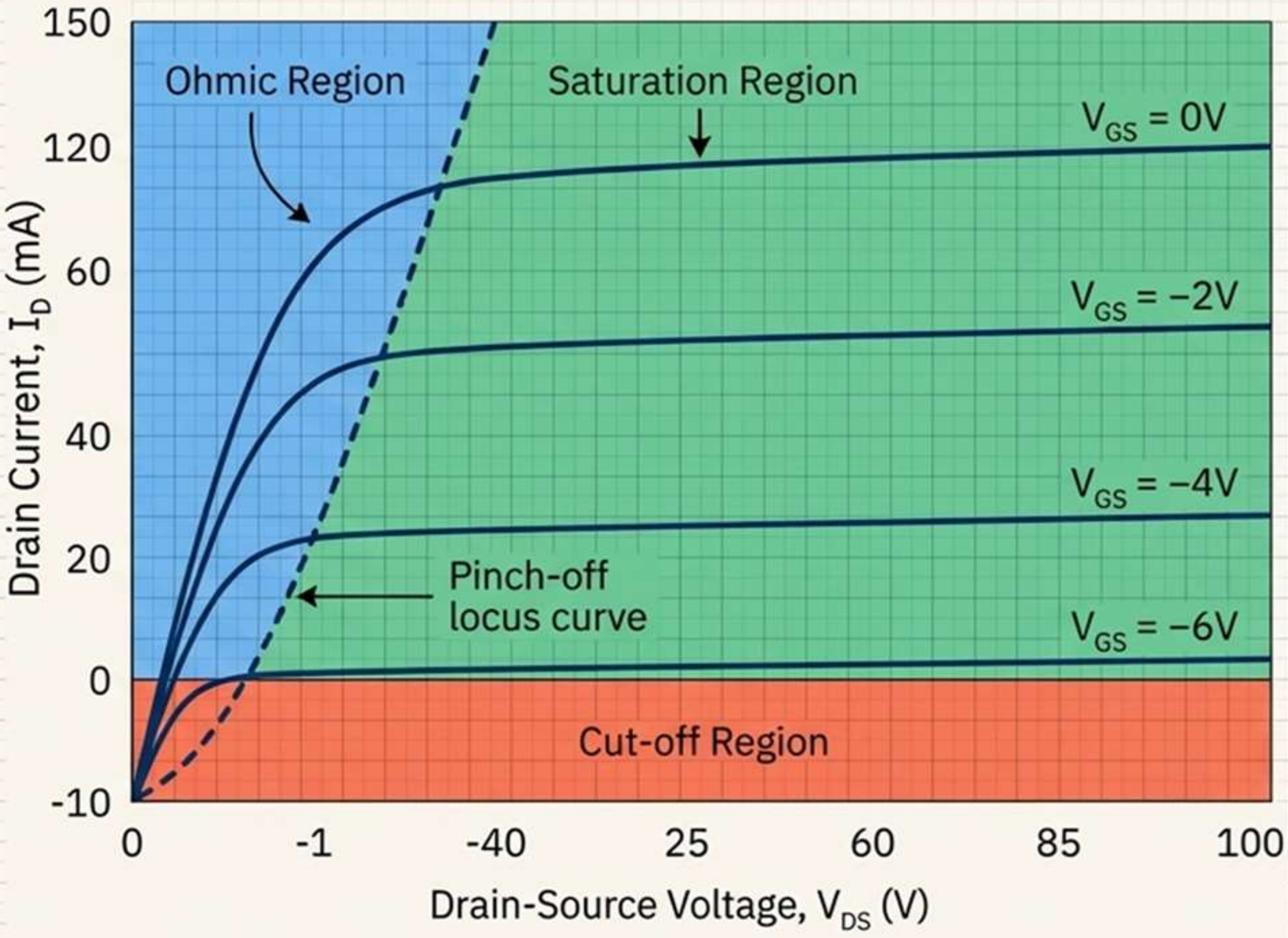
- **Condition:** $V_{DS} \geq |V_{GS} - V_P|$
- **Behavior:** Drain current (I_D) is constant, independent of V_{DS}. The ideal region for signal amplification.

Cut-Off Region

- **Condition:** $V_{GS} \leq V_P$
- **Behavior:** Channel is completely pinched off. Current is zero. Device acts as an open switch.

Output Characteristics: The Drain Curve

Mapping the precise relationship between voltage and current across operating regions.



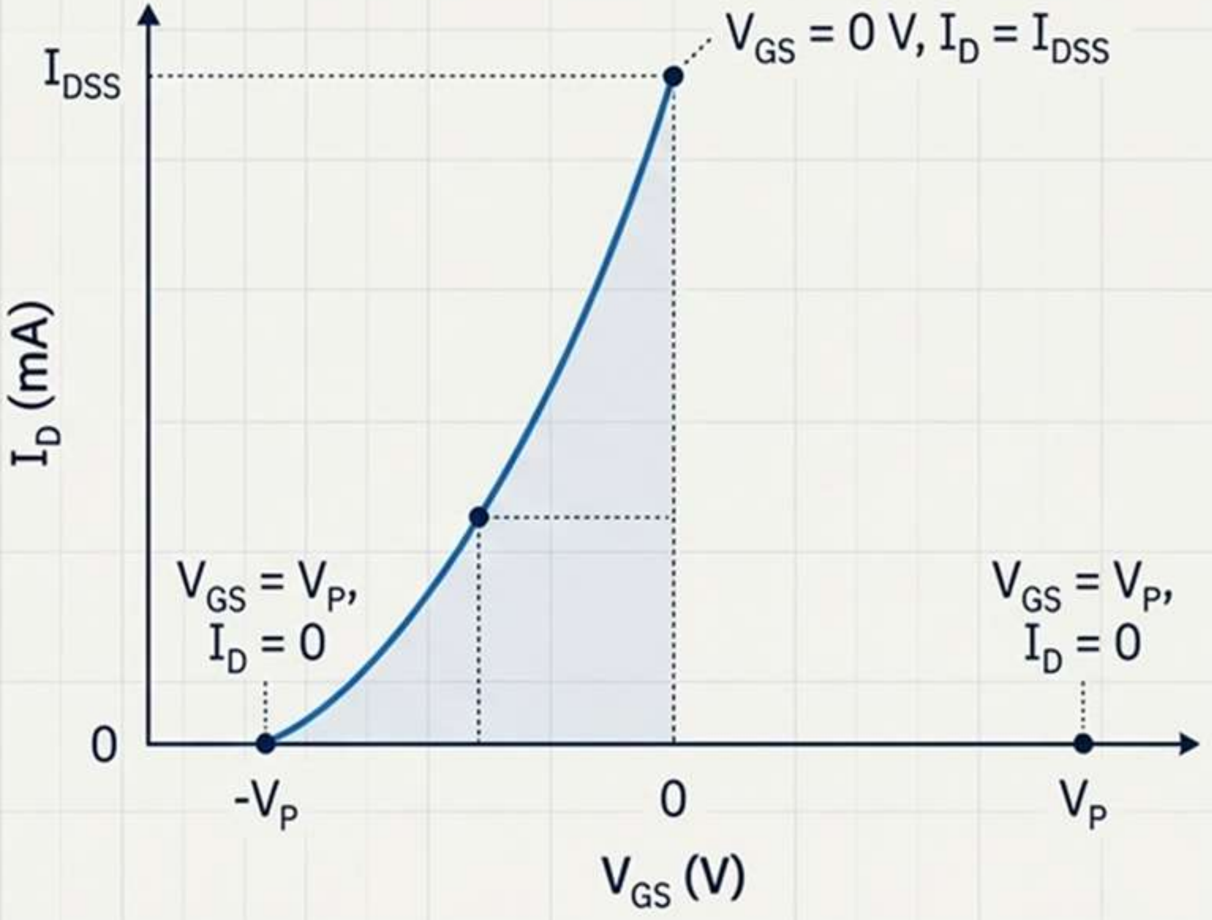
Output characteristics of JFET

Terminologies involved in output characteristics of JFET:

- **Saturation region:** In this region, the JFET operates with low V_{ds}, and the current is constant. The current is controlled by the gate source voltage (V_{gs}).
- **Ohmic region:** JFET becomes an ohmic region with increasing VDS. The drain current increases with V_{ds}.
- **Pinched off region:** By increasing the V_{DS}, it can lead to a pinch of region; in this region, the channel narrows and the drain current becomes independent of the V_{DS}.
- **Breakdown Region:** As the voltage of drain source becomes very high then the JFET channels gets breakdown and current flows in an uncontrolled manner.

Transfer Characteristics & Shockley's Equation

The mathematical heart of the device.



$$I_D = I_{DSS} \times (1 - V_{GS}/V_P)^2$$

- I_D : Actual drain current
- I_{DSS} : Maximum saturation current (when $V_{GS} = 0$)
- V_P : Pinch-off voltage (channel is fully depleted)
- V_{GS} : Gate-to-Source voltage (the control input)

Transfer characteristics of a JFET

The transfer characteristics of a JFET plotted between the drain current (Id) and drain source voltage (V_{ds}).

- It can be determined by keeping the V_{ds} constant and drain current can be observed by changing the gate source voltage. So we can observe that when the gate source voltage Vgs is increased, the drain current Id decreases.
- When the drain source voltage is constant, it can be observed that the value of the drain current varies inversely with respect to the gate source voltage.
- The above transfer characteristics curve of JFET is described below; it can be observed that the value of drain current varies inversely with respect to gate-source voltage (V_{gs}) when the drain-source voltage is constant.

The Vitals: Key Electrical Parameters

I_{DSS}

Zero Gate-Bias Drain Current

Defines the absolute maximum channel conduction.

Typical range: 1–100 mA.

V_P

Pinch-off Voltage

The threshold where the channel completely closes.

Typical range: -1V to -10V.

g_m

Transconductance

The voltage-to-current gain (dI_D / dV_{GS}). Peaks at $V_{GS} = 0$.

Typical values: 1000–10000 µS.

R_{in}

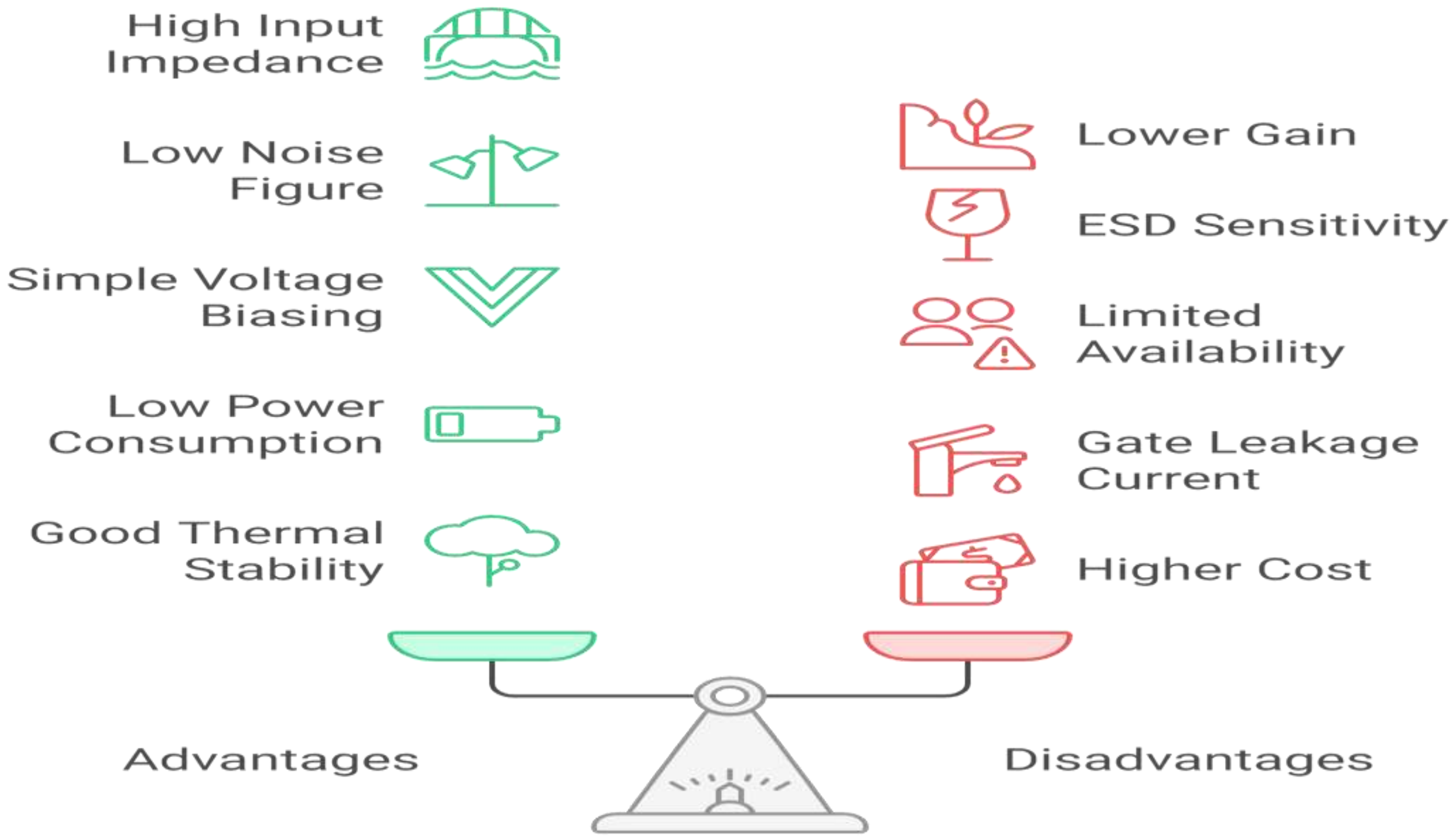
SUPERPOWER

Input Impedance

The JFET's superpower. The AC resistance looking into the gate.

Typically > 100 kΩ (often > 10^9 Ω).

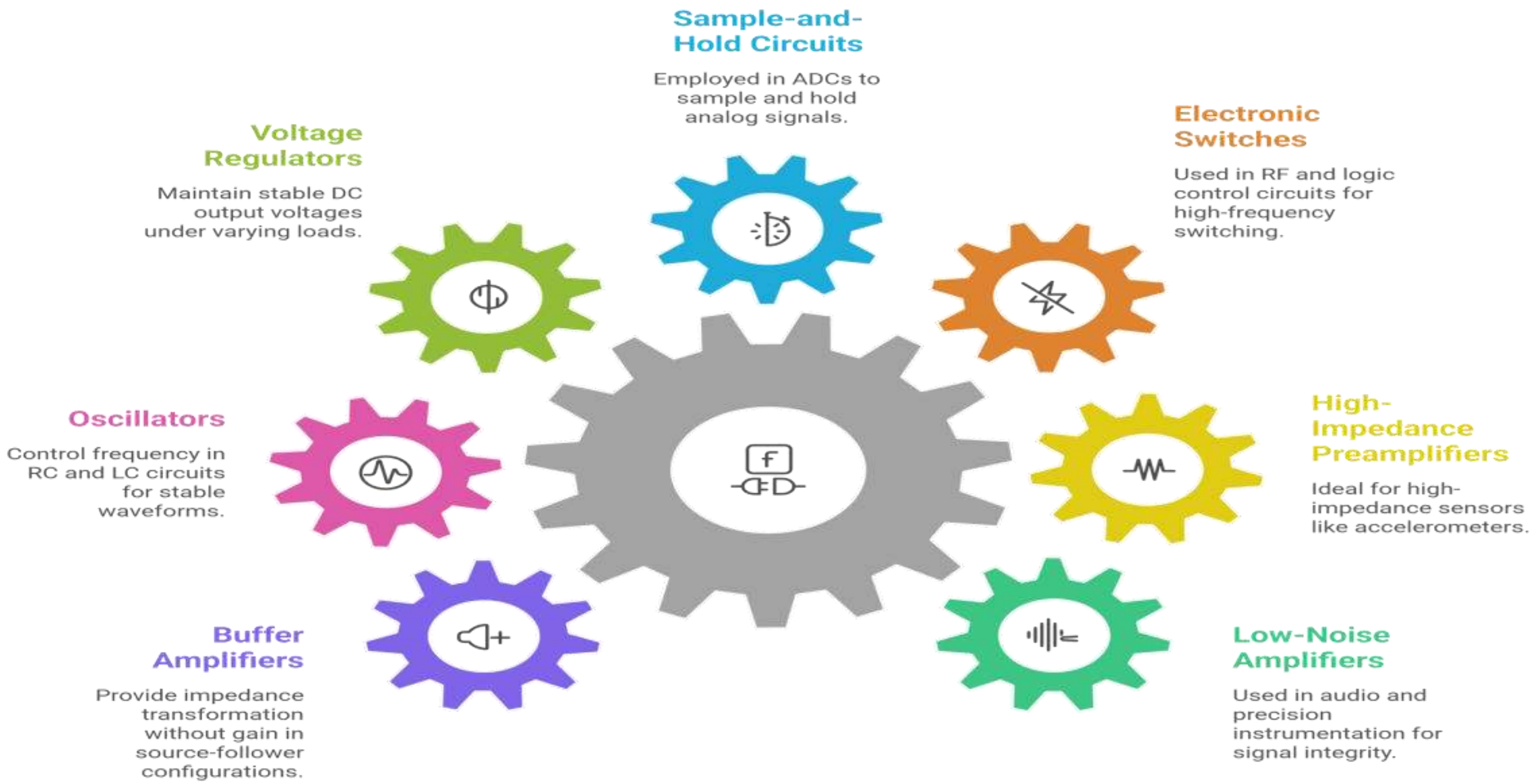
Trade Off’s



High Input Impedance
Low Noise Figure
Simple Voltage Biasing
Low Power Consumption
Good Thermal Stability
Lower Gain
ESD Sensitivity
Limited Availability
Gate Leakage Current
Higher Cost
Advantages
Disadvantages

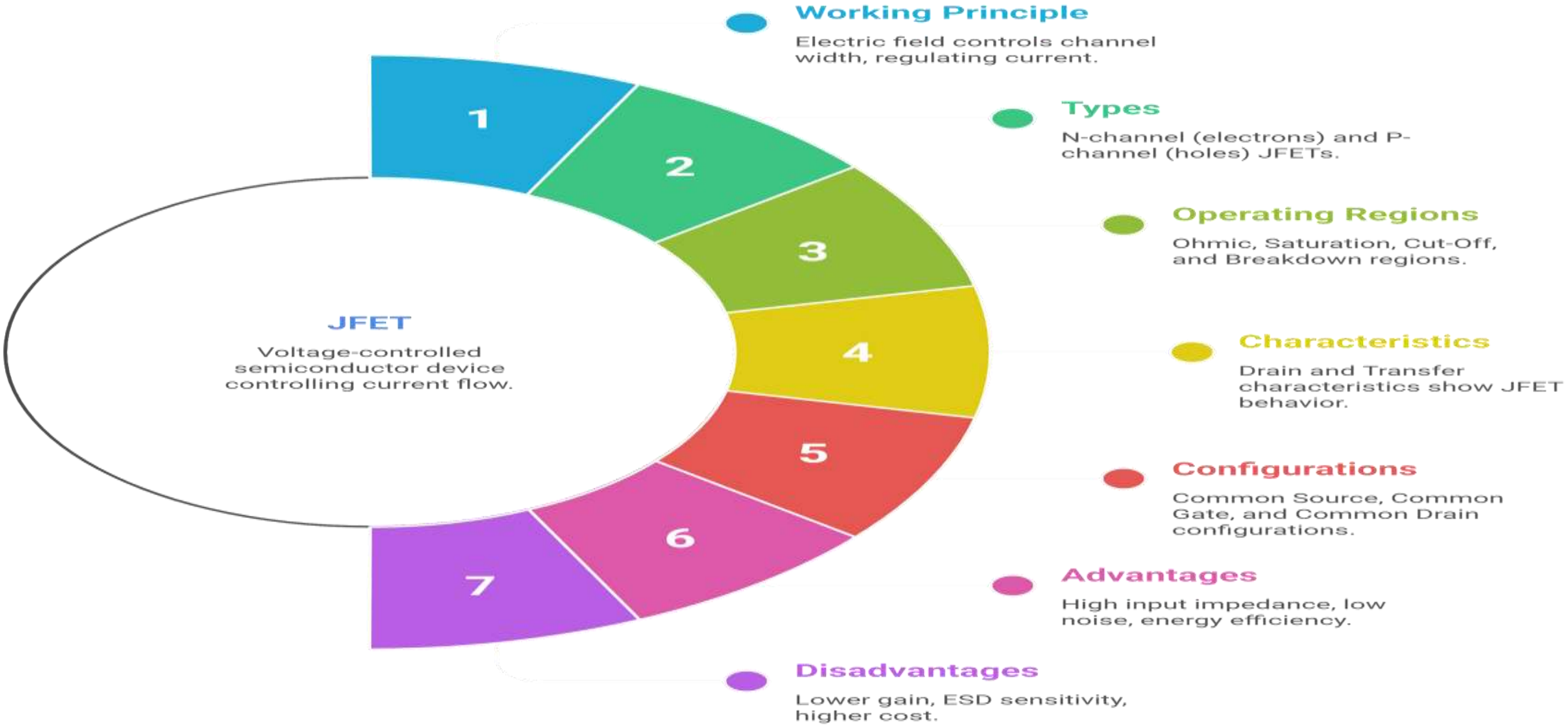
Applications of JFET

DT-IDEATE



Summary

Let's Summarize



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Thank You