UNIT –I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES

1. a)Explain different steps involved in preparation CMOS using twin tub process.[7M]
   b)Define Figure of merit and $g_{ds.}$ [3M]
2. Derive the relation between drain to source current I_{ds} VS drain to source voltage V_{ds}in non-saturated and saturated region. [10M]
3. a)Compare CMOS and Bi-CMOS. [6M]
   b)Write short notes on latch-up in CMOS circuits [4M]
4. Determine the Pull-up and Pull-down ratio of for NMOS inverter through one (or) more pass transistors. [10M]
5. (a) What is meant by body effect? [5M]
   (b) Explain a Bi-CMOS inverter with a neat sketch. [5M]
6. a)Define the term Threshold voltage of MOSFET and explain its significance. [5M]
   b)Briefly discuss about the pass transistor [5M]
7. a)Compare NMOS and CMOS technology. [5M]
   b)Derive the expression for ZPU/ZPD. [5M]
8. a)Illustrate the main steps in a typical N-WELL process. [7M]
   b)Explain the NMOS depletion mode transistor. [3M]
9. a)Explain about the Structure of NMOS transistor. [7M]
   b)Explain the operation of CMOS inverter with a logic diagram [3M]
10. a)Explain about PASS transistor with neat sketch [5M]
    b)Define electrical properties of MOS circuits. [5M]

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UNIT –II

LAYOUT DESIGN AND TOOLS\LOGIC GATES & LAYOUTS

1. a)Explain how stick diagrams can be used for layout diagrams. [7M]
   b)Discuss the wiring capacitances [5M]
2. (a) Explain about static complementary gates. [5M]
   (b) What are the different strategies for building low power gates? Explain. [5M]
3. (a) Differentiate switch logic and gate logic. [5M]
   (b) List the salient features of subsystem lay out. [5M]
4. (a) Explain clearly the Scalable design rules. [5M]
   (b) Explain clearly Wires and Vias in VLSI design. [5M]
5. Design the static complementary pull-up and pull-down networks for the logic expression: f(A,B,C,D)=(A+B)(C+D) [10M]
6. a)Explain switch Logic and Alternative Logic. [6M]
   b)Briefly discuss about the combinational logic functions [4M]
7. a)Explain briefly about Resistive Inter-Connect delay and RC Trees delay. [5M]
   b)Explain about driving large loads with diagram. [5M]
8. What are layout design rules? Explain the layer representations and based design rules for CMOS process. [10M]
9. (a) Implement NAND gate in NMOS technology and hence draw its stick diagram and design a layout for the stick diagram. [5M]
   (b) Discuss about the effects of scaling down the dimensions of MOS circuits and Systems. [5M]
10. Define the following terms
    (a) Speed power product. [5M]
    (b) Delay through RC transition time [5M]

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UNIT –III

COMBINATIONAL LOGIC NETWORKS\SEQUENTIAL SYSTEMS

1. a)Explain in detail about the requirements in designing logic networks using realistic interconnect models. [7M]
   b)Draw the single row layout design. [3M]
2. a)Explain briefly about power optimization. [5M]
   b)Draw the switch implementation of a multiplier. [5M]
3. (a)What are the various simulators used for combinational logic? [5M]
   (b) Write short notes on power optimization of combinational logic networks. [5M]
4. a)Briefly discuss about Fanout with diagram [5M]
   b)Explainpath delay with respect to combination networks delay. [5M]
5. a)Explain the clocking disciplines and power optimization in sequential systems. [5M]
   b)Briefly discuss about crosstalk minimization. [5M]
6. (a) Explain clearly about switch simulation. [5M]
   (b) Explain about the combinational network testing. [5M]
7. Draw the layout diagram of three input NAND gate in CMOS. [10M]
8. What is simulation? Explain about various types of simulation applied at different levels of fabrication. [10M]
9. a)With suitable examples explain about network delays combinational logic circuits. [5M]
   (b) Implement an ‘n-bit’ shift register and explain its operation over one clock cycle.[5M]
10. a)Discuss briefly about standard cell layout design. [5M]
    b)Briefly explain the block diagram of phase locked loop for clock generation. [5M]

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UNIT-IV

FLOOR PLANNING AND ARCHITECTURE DESIGN

1	a)Briefly discuss about floor planning methods.	[5M]
	b)Draw and explain the block placement and channel definition.	[5M]
2	a)Write a short notes on global routing	[5M]
	b)Explain the concept of switch box routing	[5M]
3	a)Discuss about different floor planning tips.	[5M]
	b)Write a short notes on design validation.	[5M]
4	a)Explain about placement and routing at chip level design.	[5M]
	b)Explain about architecture testing.	[5M]
5	a)Discuss about off-chip connections and packages	[7M]
	b)Draw and explain the power line inductance	[3M]
6	a)Draw and explain the I/O architecture with a neat sketch.	[5M]
	b)Explain the concept of pad design with a diagram.	[5M]
7	Explain the concept of register transfer design with data path control architecture.	[10M]
8	With a flow chart explain the concept of ASM chart design.	[10M]
9	a)Discuss high level synthesis.	[5M]
	b)Write a short notes on power down modes.	[5M]
10	a)Explain the architecture for low power with a diagram.	[5M]
	b)Write a notes on linear feedback shift register.	[5M]

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UNIT-V

INTRODUCTION TO CAD SYSTEM AND CHIP DESIGN

1	Write about the following	
	a)Hardware-software co-design	[5M]
	b)Floor planning methods	[5M]
2	a)Write a short notes on layout synthesis	[5M]
	b)Discuss about global routing	[5M]
3	a)With an example give the method involved in the chip design.	[7M]
	b)Briefly discuss about CAD system.	[3M]
4	a)Explain about system on chips and embedded CPUs.	[5M]
	b)Write a notes on logic synthesis.	[5M]
5	With a diagram explain about detailed routing method.	[10M]
6	a)Explain the timing analysis and optimization process	[5M]
	b)Write about test generation pattern.	[5M]
7	a)Explain the technology independent logic optimization.	[7M]
	b)Draw the diagram of irredundant-reduced cycle.	[3M]
8	a)Write a short notes on sequential machine optimizations.	[5M]
	b)Explain about scheduling ad binding.	[5M]
9	a)Write about switch level simulation	[7M]
	b)Write a short notes on chip level placement.	[3M]
10	Explain about technology dependent logic optimization.	[10M]

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