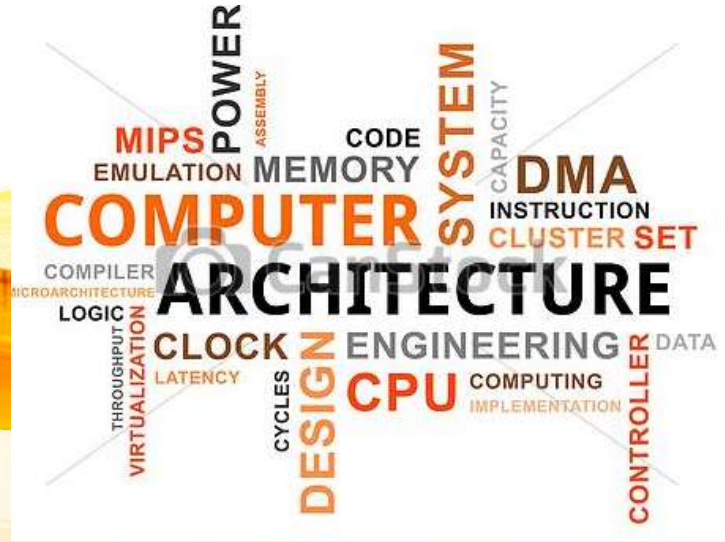
UNIT III
PROCESSOR AND PIPELINING

Fundamental concepts – Execution of a complete instruction – **Multiple bus organization** – Hardwired control – Micro programmed control – Pipelining: Basic concepts – Data hazards – Instruction hazards – Influence on Instruction sets – Data path and control consideration.



Recap the previous Class

Multiple-Bus Organization

• Allow the contents of two different registers to be accessed simultaneously and have their contents placed on buses A and B.

• Allow the data on bus C to be loaded into a third register during the same clock cycle.

• Incrementer unit.

• ALU simply passes one of its two input operands unmodified to bus C

→ control signal: R=A or R=B

- General purpose registers are combined into a single block called registers.
- 3 ports,2 output ports –access two different registers and have their contents on buses A and B
- Third port allows data on bus c during same clock cycle.
- Bus A & B are used to transfer the source operands to A & B inputs of the ALU.
- ALU operation is performed.
- The result is transferred to the destination over the bus C.

- ALU may simply pass one of its 2 input operands unmodified to bus C.
- The ALU control signals for such an operation R=A or R=B.
- Incrementer unit is used to increment the PC by 4.
- Using the incrementer eliminates the need to add the constant value 4 to the PC using the main ALU.
- The source for the constant 4 at the ALU input multiplexer can be used to increment other address such as load multiple & store multiple

Multiple-Bus Organization

- Add R4, R5, R6

Step	Action
1	PC_{out}, R=B, MAR_{in}, Read, IncPC
2	WMFC
3	MDR_{outB}, R=B, IR_{in}
4	$R4_{outA}$, $R5_{outB}$, SelectA, Add, $R6_{in}$, End

Figure 7.9. Control sequence for the instruction. Add R4,R5,R6, for the three-bus organization in Figure 7.8.

- Step 1:The contents of PC are passed

  through the ALU using R=B control signal & loaded into MAR to start a memory read operation

  At the same time PC is incrementer by 4
- Step 2:The processor waits for MFC
- Step 3: Loads the data ,received into MDR ,then transfers them to IR.
- Step 4: The execution phase of the instruction requires only one control step to complete.


Thank You