SNS COLLEGE OF TECHNOLOGY

COIMBATORE-35

DEPARTMENT OF ARTIFICIAL INTELLIGENCE

AND MACHINE LEARNING

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Course **:** 19ITT202 – Computer Organization and Architecture
Semester **:** V
Class **:** III Year B.Tech AIML
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Question Bank

UNIT I

PART A

1. Define Computer Architecture.
2. What are the five classic components of a computer?
3. What are the addressing modes?
4. State the need for indirect addressing mode. Give an example.
5. What is an instruction register?
6. Give the formula for CPU execution time for a program.
7. How to represent instruction in a computer system?
8. Distinguish between auto increment and auto decrement addressing mode.
9. What is instruction set architecture?
10. List the various elements of instruction.
11. What are the functions of control unit?
12. What is a Bus? List out its functional groups.
13. What is Bus arbitration?
14. Define memory space.
15. What is straight line sequencing?
16. Define branching.
17. What are conditional codes?
18. What do you mean by response time?
19. List various instruction formats with example.
20. Define throughput and throughput rate.

PART B

1. Explain the various components of computer System with neat diagram.
2. Discuss in detail the various measures of performance of a computer.
3. Explain briefly on instruction set and its types with an example of each type.
4. Explain with an example about the operations and operands of the computer hardware.
5. Define Addressing mode and explain the basic addressing modes with an example for each.
6. Discuss about the various techniques to represent instructions in a computer system.
7. State the CPU performance equation and discuss the factors that affect the performance.

UNIT II

PART A

1. What are the rules to perform addition on floating point numbers?
2. Subtract (11010)2-(10000)2 using 1's complement and 2's complement method.
3. Add 6_{10} to 7_{10} in binary and Subtract 6_{10} from 7_{10} in binary.
4. What is an overflow? When does it occur?
5. Define ALU.
6. What are the overflow/underflow conditions for floating point addition and subtraction?
7. State the representation of double precision floating point number.
8. Define Little Endian arrangement.
9. List out the advantages of carry-look ahead adder.
10. Discuss the role of booth's algorithm in the design of fast multiplier.
11. Define floating point single and double precision standard.
12. What is 2's complement of numbers?
13. What is half adder?
14. What is full adder?
15. Give the full – adder circuit truth table.
16. What is a Carry Look-ahead adder?
17. What is fast multiplication?
18. How bit pair recording of multiplier speeds up the multiplication process?
19. What is scientific notation and normalization? Give an example.
20. List the two division algorithms.

PART B

1. Explain briefly about floating point addition and subtraction algorithms.
2. Explain briefly about carry-look ahead adder and also give the expression for full adder circuit to show carry generation and propagation.
3. i) Draw the Multiplication hardware diagram and List the steps of Multiplication algorithm.
   ii) Apply the Multiplication algorithm for the binary values 1010 & 1011.
4. Explain booth multiplication algorithm in detail and calculate 8 * 4 using booth multiplication algorithm.
5. Draw and Explain the flowchart of restoring and non restoring division algorithm.
6. Draw the logic circuit for restoring division algorithm and solve the given problem Dividend=24 and Divisor= 3.
7. Divide (12)10 by (3)10 using the restoring and non-restoring division algorithm with step by step intermediate results and explain.

UNIT III

PART A

1. What is meant by data path element?
2. Mention the various phase in executing an instruction.
3. What is meant by pipeline bubble?
4. List out the main elements in building a datapath.
5. What are the advantages of pipelining?
6. What are the elements required by the different classes of instruction.
7. What are the five steps in MIPS instruction execution?
8. What is meant by forwarding?
9. What are exceptions and interrupts?
10. What is a hazard? What are its types?
11. What is meant by branch prediction?
12. What is a branch prediction buffer?
13. Name the control signals required to perform arithmetic operations.
14. Define data hazard. Give an example for data hazard.
15. What are the instructions set available in MIPS architecture?
16. What is meant by program counter?
17. What are the units needed to implement MIPS load and store instructions?
18. What are the ways in which pipelining can be implemented?
19. What are the steps required for a pipelinened processor to process the instruction?
20. What is meant by dynamic branch prediction?

PART B

1. Explain the MIPS instructions and its implementation with neat sketch.
2. Explain in detail the operation of the data path and its control.
3. Explain the pipeline hazard in detail.
4. Explain how the instruction pipeline works? What are the various situations where an instructionpipeline can stall?
5. Explain the methods for dealing the data and control hazards.
6. Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.
7. Explain in detail how exceptions are handled in MIPS architecture.

UNIT IV

PART A

1. What are the temporal and spatial localities of references?
2. Draw the structure of memory hierarchy.
3. What are the various memory technologies?
4. Differentiate SRAM from DRAM.
5. What is meant by address mapping?
6. What is cache memory?
7. What are the methods used to improving cache performance?
8. State the advantages of virtual memory.
9. Point out how DMA can improve I/O speed.
10. Define memory interleaving.
11. What is direct-mapped cache?
12. Summarize the sequence of events involved in handling an interrupt request from a single device.
13. Differentiate memory mapped I/O and I/O mapped I/O.
14. What is the purpose of dirty/modified bit in cache memory?
15. What are the steps to be taken in an instruction cache miss?
16. What is meant by virtual memory?
17. Define hit ratio.
18. Define hit rate and miss rate.
19. What are the two I/O interfacing techniques?
20. What is TLB?

PART B

1. Explain in detail about memory technologies & Memory Hierarchy with neat diagram.
2. Describe the basic operations of cache in detail with diagram.
3. Discuss the various mapping schemes used in cache design.
4. What is cache memory? How to improve the cache performance? Discuss.
5. Discuss DMA controller with block diagram.
6. Discuss the steps involved in the address translation of virtual memory with necessary block diagram.
7. Design and explain parallel priority interrupt hardware for a system with eight interrupt sources.

UNIT V

PART A

1. What is Parallelism? List out the goals of parallelism.
2. What is meant by ILP?
3. What is multiple issue? Write any two approaches.
4. What is multi-threading?
5. Difference between fine-grained multi-threading and coarse grained multi- threading.
6. What are the two main approaches to hardware multithreading?
7. Distinguish implicit multi-threading and explicit multi-threading.
8. What is Flynn's classification?
9. Define super scalar processor.
10. What is meant by task level parallelism?
11. What is a multicore microprocessor?
12. What are the challenges includes in parallel programming?
13. What are the advantages of SIMD?
14. What is MISD?
15. What is MIMD?
16. Write the advantages and disadvantages of fine grainedmultithreading.
17. Write the advantages and disadvantages of coarse grained multithreading.
18. What is simultaneous multithreading?
19. What is static multiple issue?
20. What is dynamic multiple issue?

PART B

1. Explain instruction level parallel processing. State the challenges of parallel processing.
2. Discuss the challenges in parallel processing with necessary examples.
3. Explain with diagrammatic illustration Flynn's classification.
4. Describe Simultaneous Multithreading (SMT) with an example.
5. Discuss shared memory multiprocessor with a neat diagram.
6. Explain the different types of multithreading.
7. Write short notes on (a) Hardware Multi-threading (b) Multicore processors.