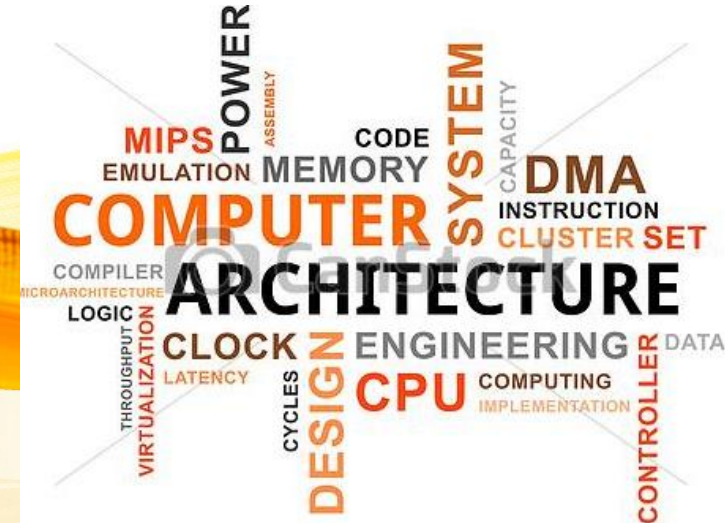# UNIT V
I/O ORGANIZATION AND PARALLELISM

Accessing I/O devices – Interrupts – **Direct Memory Access** - Buses– Interface circuits - Standard I/O Interfaces (PCI, SCSI, USB)–Instruction Level Parallelism : Concepts and Challenges – Introduction to multicore processor Graphics Processing Unit.

Recap the previous Class

Direct Memory Access (DMA)

- For I/O transfer, Processor determines the status of I/O devices, by

    – Polling

    – Waiting for Interrupt signal

- Considerable overhead is incurred in above I/O transfer processing

- To transfer large blocks of data at high Speed, between EXTERNAL devices & Main Memory, DMA approach is often used

- DMA controller allows data transfer directly between I/O device and Memory, with minimal intervention of processor.

Direct Memory Access (DMA)

- DMA controller acts as a Processor, but it is controlled by CPU

- To initiate transfer of a block of words, the processor sends the following data to controller

  - The starting address of the memory block

  - The word count

  - Control to specify the mode of transfer such as read or write

  - A control to start the DMA transfer

- DMA controller performs the requested I/O operation and sends a interrupt to the processor upon completion

|	31	30		1	0
Status and Control	IRQ	IE		R/W	Done

Starting address

Word count

In DMA interface

- First register stores the starting address
- Second register stores Word count
- Third register contains status and control flags

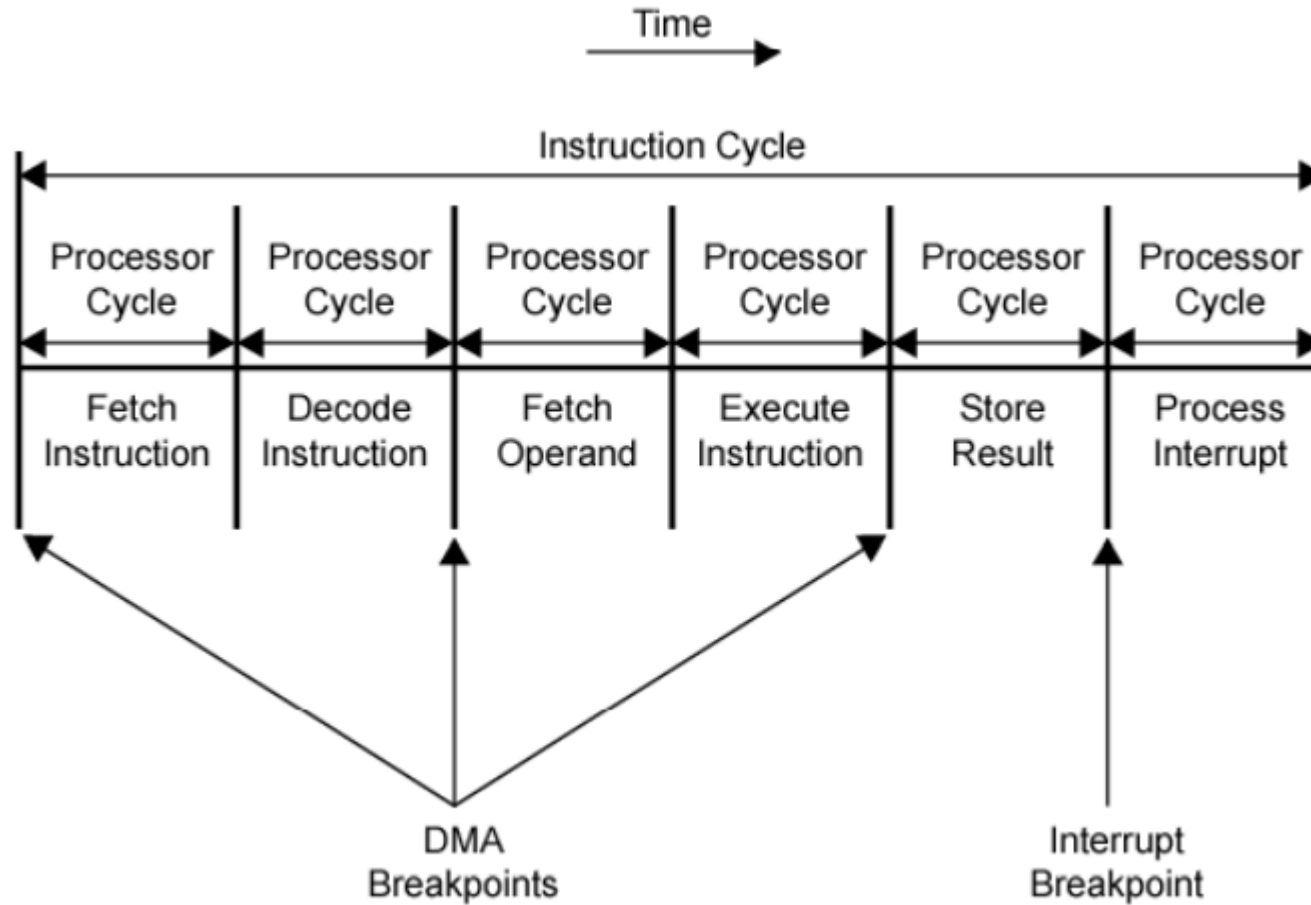| Bits and Flags	1	0
R/W	READ	WRITE
Done	Data transfer finishes	
IRQ	Interrupt request	
IE	Raise interrupt (enable) after Data Transfer	

Use of DMA Controller in a computer system
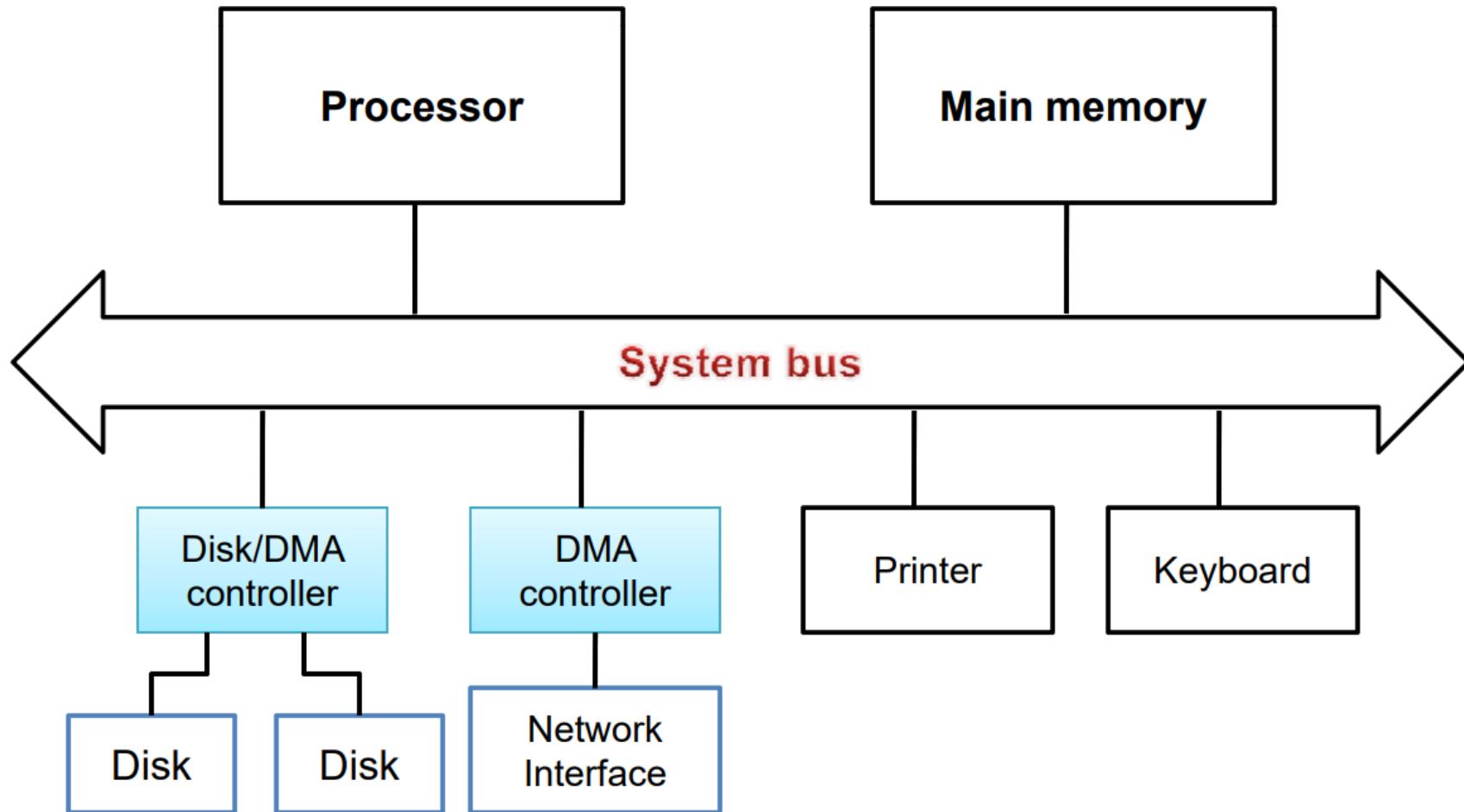
- Memory accesses by the processor and DMA Controller are interwoven
- DMA devices have higher priority then processor over BUS control
- **Cycle Stealing**:- DMA Controller "steals" memory cycles from processor, though processor originates most memory access.
- **Block or Burst mode**:- The DMA controller may given exclusive access to the main memory to transfer a block of data without interruption
- **Conflicts in DMA**:

    - Processor and DMA,

    - Two DMA controllers, try to use the Bus at the same time to access the main memory

Thank You