Reg.No: | | | | | | | |

SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
Coimbatore – 641 035.

B.E / B.Tech – Internal Assessment Exam- III
Academic Year 2023-2024 (ODD)
FIFTH SEMESTER (REGULATION R2019)

A

19ITT202 – COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 1.5 HOURS **MAXIMUM MARKS: 50**

ANSWER ALL QUESTIONS

PART A — (5 x 2 = 10 Marks)

1.	Differentiate SRAM from DRAM	CO4	UND
2.	What is memory access time?	CO4	REM
3.	Define read hit and write miss.	CO4	REM
4.	What is memory mapped I/O?	CO5	UND
5.	Mention the difference between subroutine and an Interrupt Subroutine.	CO5	UND

PART- B (2 x 13 = 26 Marks , 1*14=14 Marks)

6.	(a)	Describe the basic concepts of Semiconductor RAM memories in detail with diagram.	13	CO4	UND
		(OR)			
	(b)	Discuss the various mapping schemes used in cache design	13	CO4	UND
7.	(a)	Discuss about Read Only Memories (ROM)	13	CO4	UND
		(OR)			
	(b)	Discuss DMA controller with block diagram.	13	CO5	REM
8.	(a)	Explain about interrupts.	14	CO5	UND
	(b)	Summarize in detail about synchronous and asynchronous bus	14	CO5	UND

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