

Timing Diagram

Timing Diagram is a graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states.

Instruction Cycle:

The time required to execute an instruction is called instruction cycle.

Machine Cycle:

The time required to access the memory or input/output devices is called machine cycle.

T-State:

- ü The machine cycle and instruction cycle takes multiple clock periods.
- ü A portion of an operation carried out in one system clock period is called as T-state.

1 Machine cycles of 8085

The 8085 microprocessor has 5 (seven) basic machine cycles. They are

- ü Opcode fetch cycle (4T)
- ü Memory read cycle (3 T)
- ü Memory write cycle (3 T)
- ü I/O read cycle (3 T)
- ü I/O write cycle (3 T)

Time period, $T = 1/f$; where $f =$ Internal clock frequency

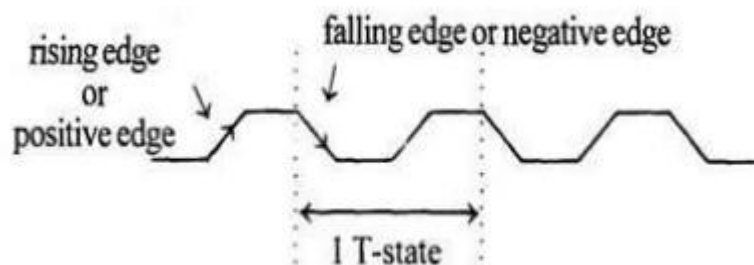


Fig 1.7 Clock Signal

Signal 1.Opcode fetch machine cycle of 8085 :

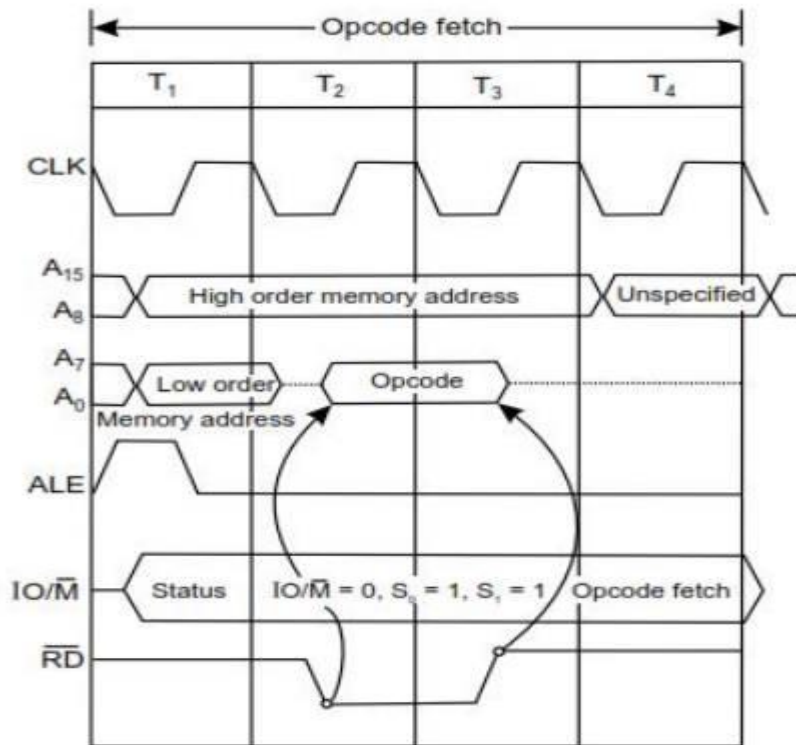


Fig 1.8 Opcode fetch machine cycle

- ü Each instruction of the processor has one byte opcode.
- ü The opcodes are stored in memory. So, the processor executes the opcode fetch machine cycle to fetch the opcode from memory.
- ü Hence, every instruction starts with opcode fetch machine cycle.
- ü The time taken by the processor to execute the opcode fetch cycle is 4T.
- ü In this time, the first, 3 T-states are used for fetching the opcode from memory and the remaining T-states are used for internal operations by the processor.

2. Memory Read Machine Cycle of 8085:

- ü The memory read machine cycle is executed by the processor to read a data byte from memory.
- ü The processor takes 3T states to execute this cycle.

The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle.

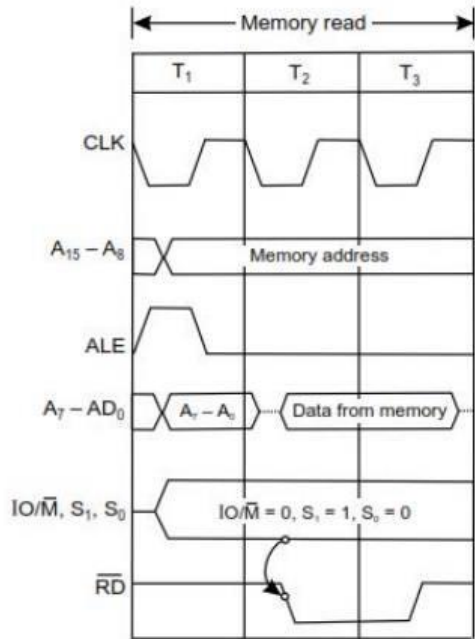


Fig 1.9 Memory Read Machine Cycle

Cycle 3. Memory Write Machine Cycle of 8085

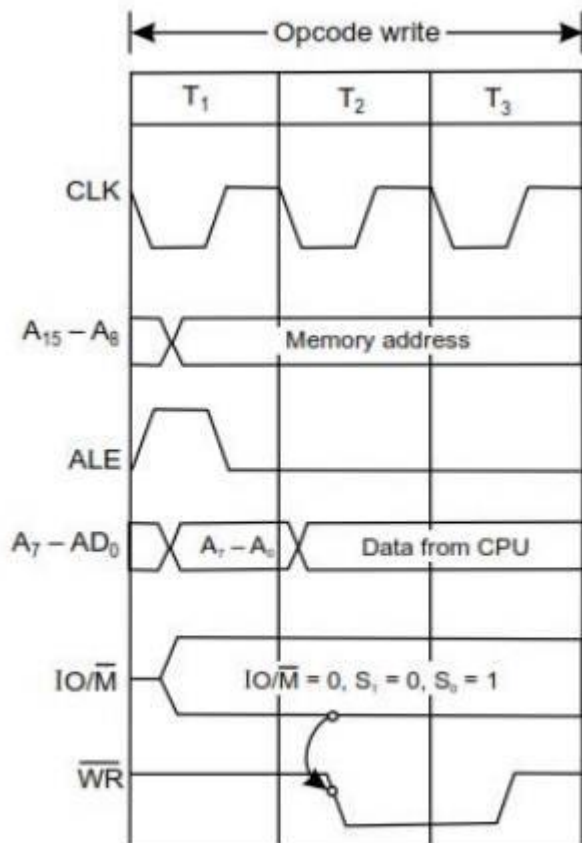


Fig 1.10 Memory Write Machine Cycle

- ü The memory write machine cycle is executed by the processor to write a data byte in a memory location.
- ✓ The processor takes, 3T states to execute this machine cycle.

4. I/O Read Cycle of 8085

- ü The I/O Read cycle is executed by the processor to read a data byte from I/O port or from the peripheral, which is I/O, mapped in the system.
- ü The processor takes 3T states to execute this machine cycle.
- ü The IN instruction uses this machine cycle during the execution.

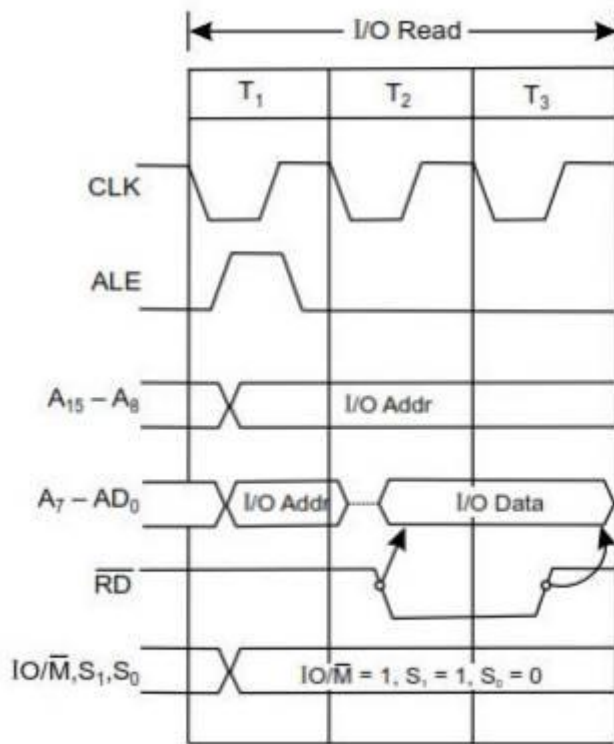


Fig 1.11 I/O Read Cycle

Cycle 1.4.2 Timing diagram for STA 526AH

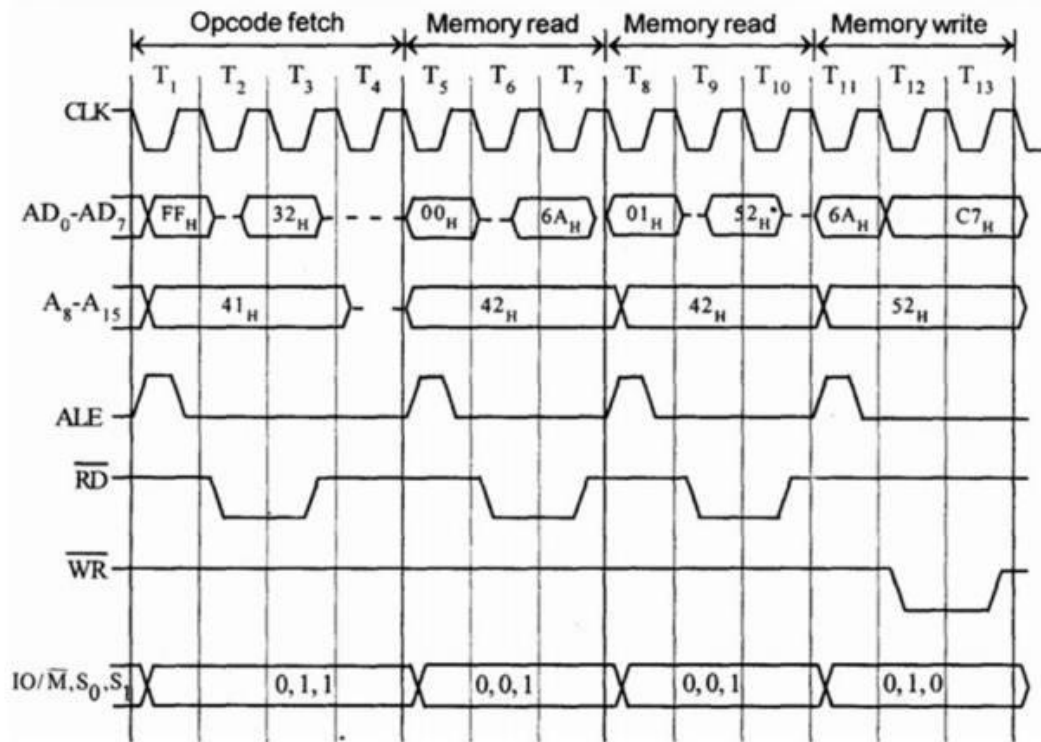


Fig 1.12 Timing Diagram for STA 526A H

Address	Mnemonics	Op code
41FF	STA 526AH	32H
4200		6AH
4201		52H

- ü STA means Store Accumulator -The contents of the accumulator is stored in the specified address (526A).
- ü The opcode of the STA instruction is said to be 32H. It is fetched from the memory 41FFH (see fig). - OF machine cycle
- ü Then the lower order memory address is read (6A). - Memory Read Machine Cycle
- ü Read the higher order memory address (52).- Memory Read Machine Cycle
- ü The combination of both the addresses are considered and the content from accumulator is written in 526A. - Memory Write Machine Cycle
- ü Assume the memory address for the instruction and let the content of accumulator is C7H. So, C7H from accumulator is now stored in 526A.