SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)

COIMBATORE-35

Accredited by NBA-AICTE and Accredited by NAAC – UGC with A++ Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ORGANIZATION OF CPU

INTRODUCTION

The Arm architecture is a family of reduced instruction set computing (RISC) architectures for computer processors. It is the most pervasive processor architecture in the world, with more than 280 billion Arm-based chips shipped by our partners over the past three decades in products ranging from sensors, wearables and smartphones to supercomputers. Benefits of the Arm CPU architecture include:

- Integrated security
- High performance and energy efficiency
- Large ecosystem for global support
- Pervasive across markets and locations

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The Arm CPU architecture is implemented by a wide range of microarchitectures to deliver software compatibility across a broad range of power, performance, and area points.

•The CPU architecture defines the basic instruction set, and the exception and memory models that are relied on by the operating system and hypervisor.
•The CPU microarchitecture determines how an implementation meets the architectural contract by defining the design of the processor and covering such things as: power, performance, area, pipeline length, and levels of cache.

CPU Structure

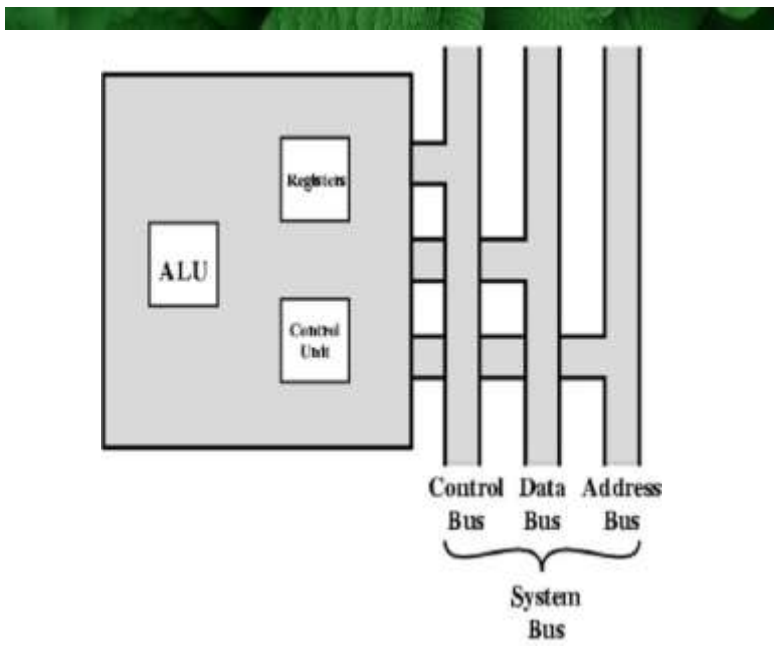
CPU must:

- Fetch instructions
- Interpret instructions
- Fetch data
- Process data
- Write data

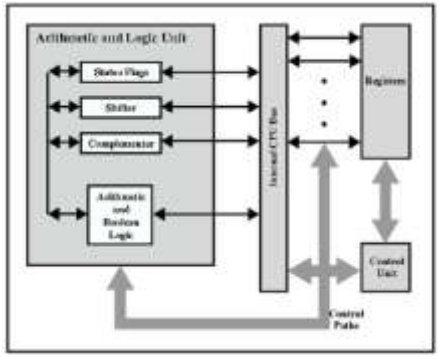
These functions require

- internal temporary storage
- remembering location of instruction to fetch next

Simplified view of CPU With System Bus



More Detailed CPU Internal Structure



Register Organization

- CPU must have some working space (temporary storage); called "registers"
- Number and function vary between processor designs
  - One of the major design decisions
  - Top level of memory hierarchy
- Two main roles

1. User Visible Registers
2. Control and Status Registers

User Visible Registers

A user visible register is simply a register than can referenced with the machine language of the processor

Four categories

- General Purpose
- Data
- Address
- Condition Codes

General Purpose Registers (1)

- May be true general purpose (all registers are the same)
  - Orthogonal to the instruction set: any register can hold any operand for any instruction (clearly not the case with X86!)
  - May be restricted (each register has special functions)
- In some machines GP registers can be used for data or addressing
- In other machines there is a separation:
  - Data
    - Accumulator and count registers
  - Addressing
    - Segment, index, autoindex registers
    - Stack pointer
- Even on machines with true general purpose registers, if there is user-visible stack addressing then the stack pointer is special- purpose

THANK YOU