



# **SNS COLLEGE OF TECHNOLOGY**

**Coimbatore-35**  
**An Autonomous Institution**



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade  
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

## **DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**19ECB211 – MICROCONTROLLER PROGRAMMING & INTERFACING**

II YEAR IV SEM

**UNIT V– ADVANCED MICROCONTROLLERS**

**TOPIC 5 – ARM Architecture**



# ARM Architecture

- The Arm architecture is the keystone of the world's largest compute ecosystem.
- It enables our partners to build their products in an efficient, affordable, and secure way.
- Arm's proven track record of delivering world-class architecture designs is reflected in the success of this diverse and ever-evolving ecosystem.
- Arm's architecture specifications are licensed by partners, who create compliant silicon chips based on them.
- With more than 125 billion devices containing Arm-based chips, our architecture empowers innovation in multiple markets enabling partner innovation



# ARM Architecture



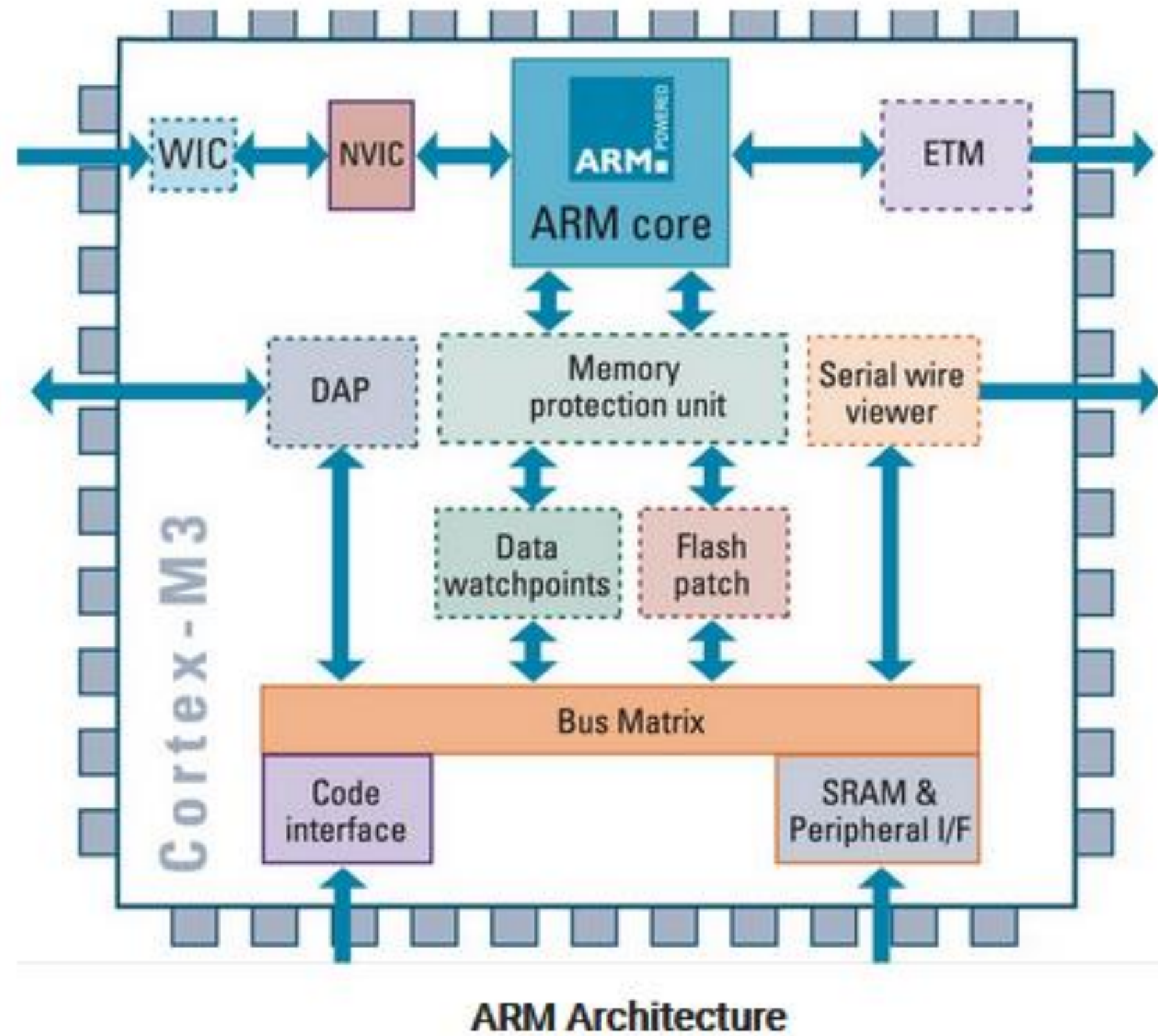
- The Arm architecture is a family of reduced instruction set computing (RISC) architectures for computer processors.
- It is the most pervasive processor architecture in the world, with billions of Arm-based devices shipped every year, from sensors, wearables and smartphones to supercomputers.

Benefits of the Arm CPU architecture include:

- Integrated security
- High performance and energy efficiency
- Large ecosystem for global support
- Pervasive across markets and locations



# ARM Architecture





# ARM Architecture



- The ARM cortex is a complicated microcontroller within the ARM family that has ARMv7 design. There are 3 subfamilies within the ARM cortex family :

ARM Cortex Ax-series

ARM-Cortex Rx-series

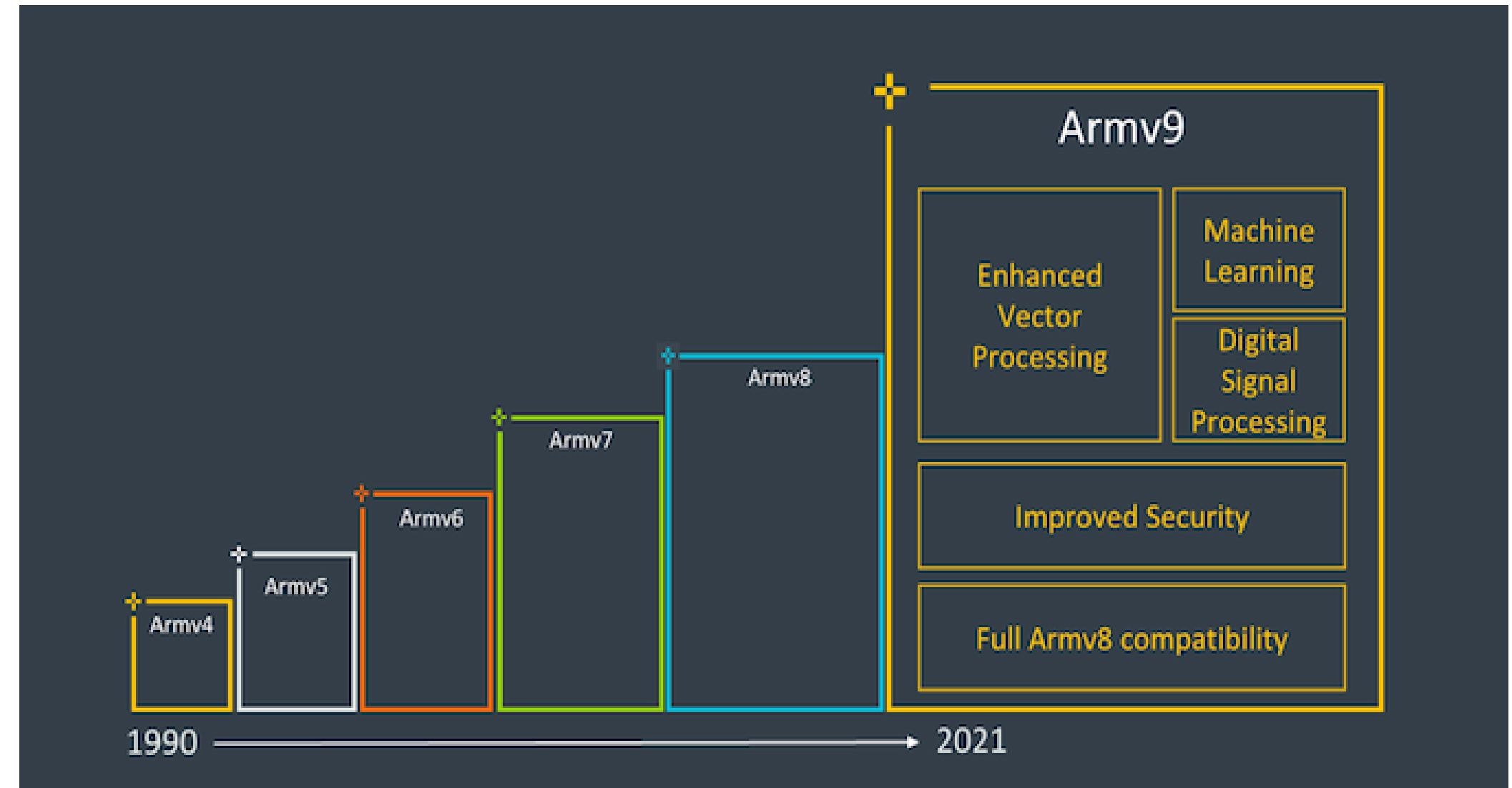
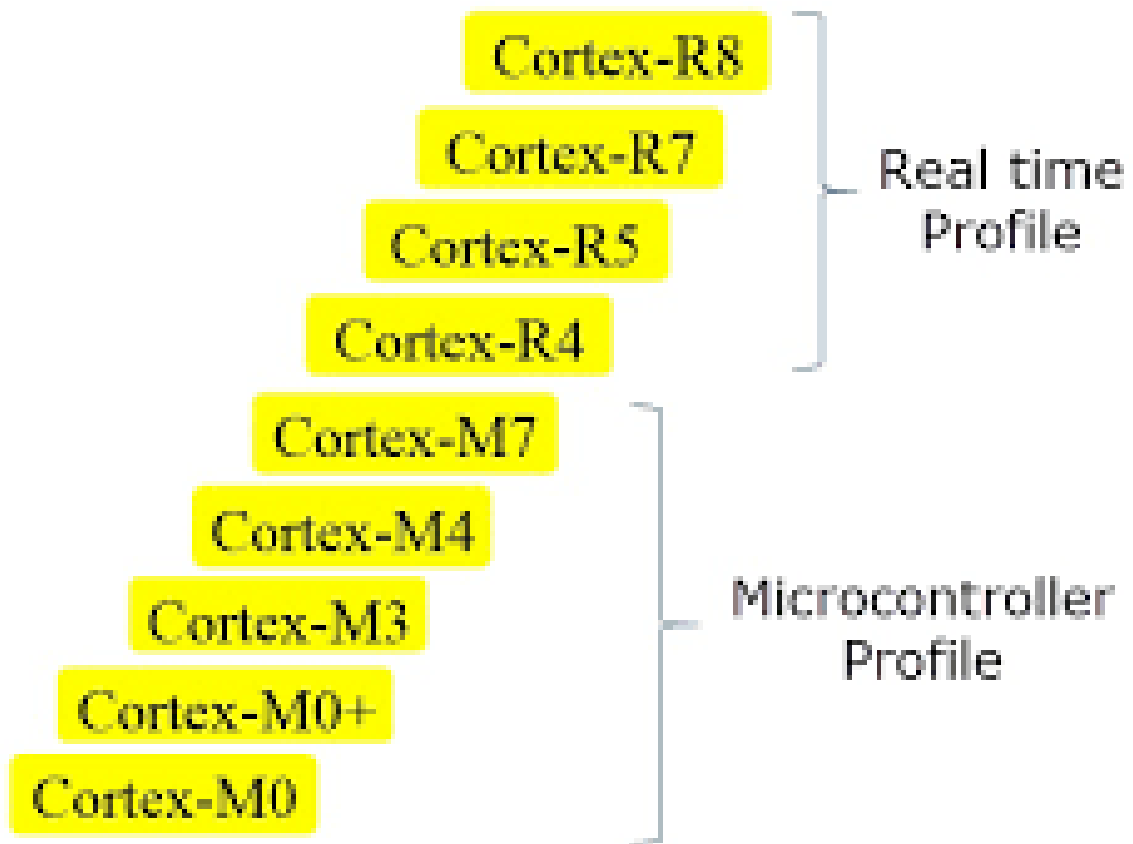
ARM-Cortex Mx-series



# ARM Architecture

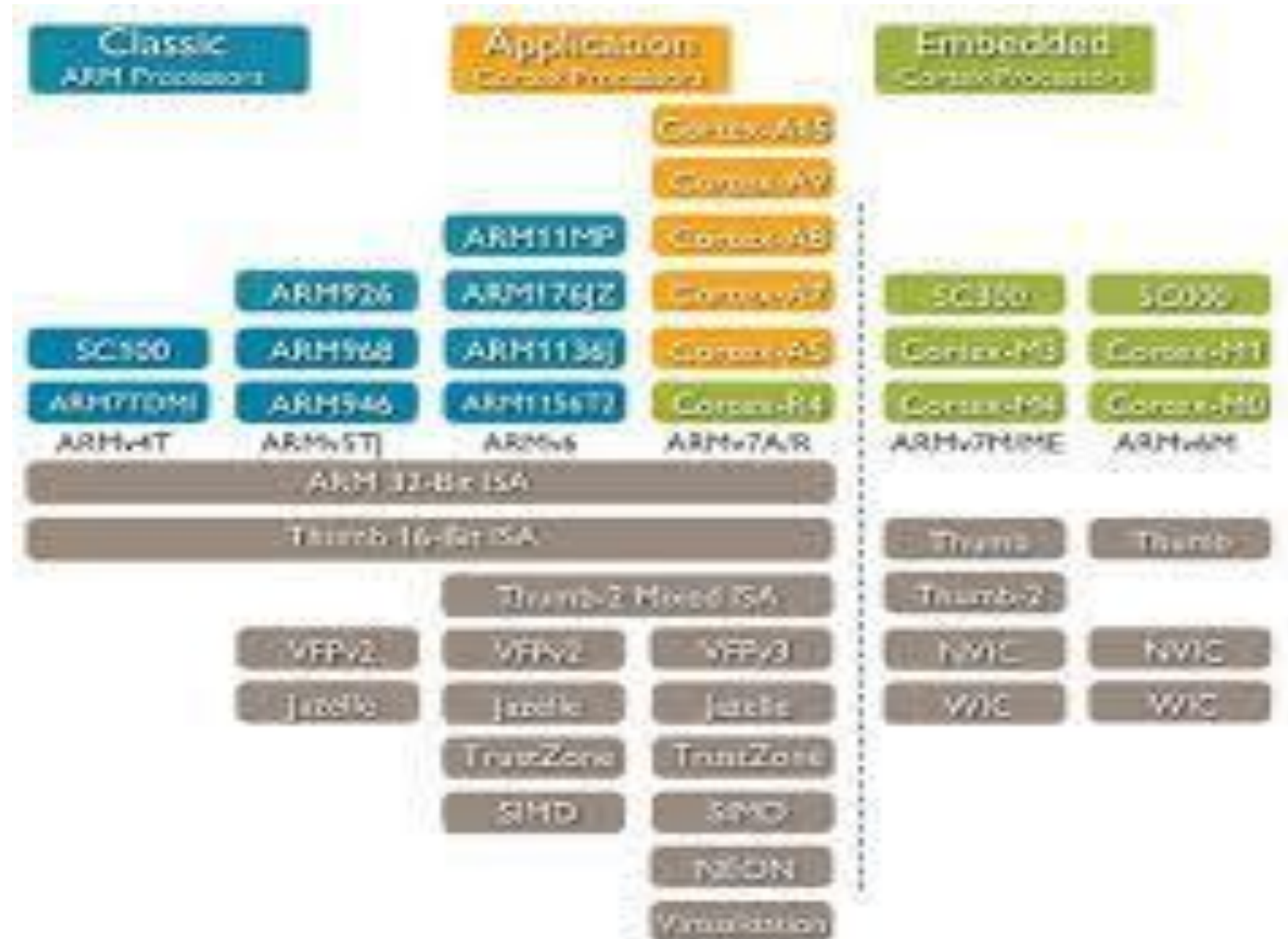


## Embedded Processors





# Which Architecture is my processor?





# Data Sizes and Instruction Sets



1. Arm is a RISC Processor
2. ARM is a 32 bit load store architecture
3. Most internal registers are 32 bits

With relation to Arm,

Word = 32 bits

Halfword = 16 bits

Doubleword = 64 bits

4. Implements two instruction sets – Arm and Thumb Instructions
  5. Older cores support 16 bit thumb instruction only.
- Maintains code density with increased feasibility.





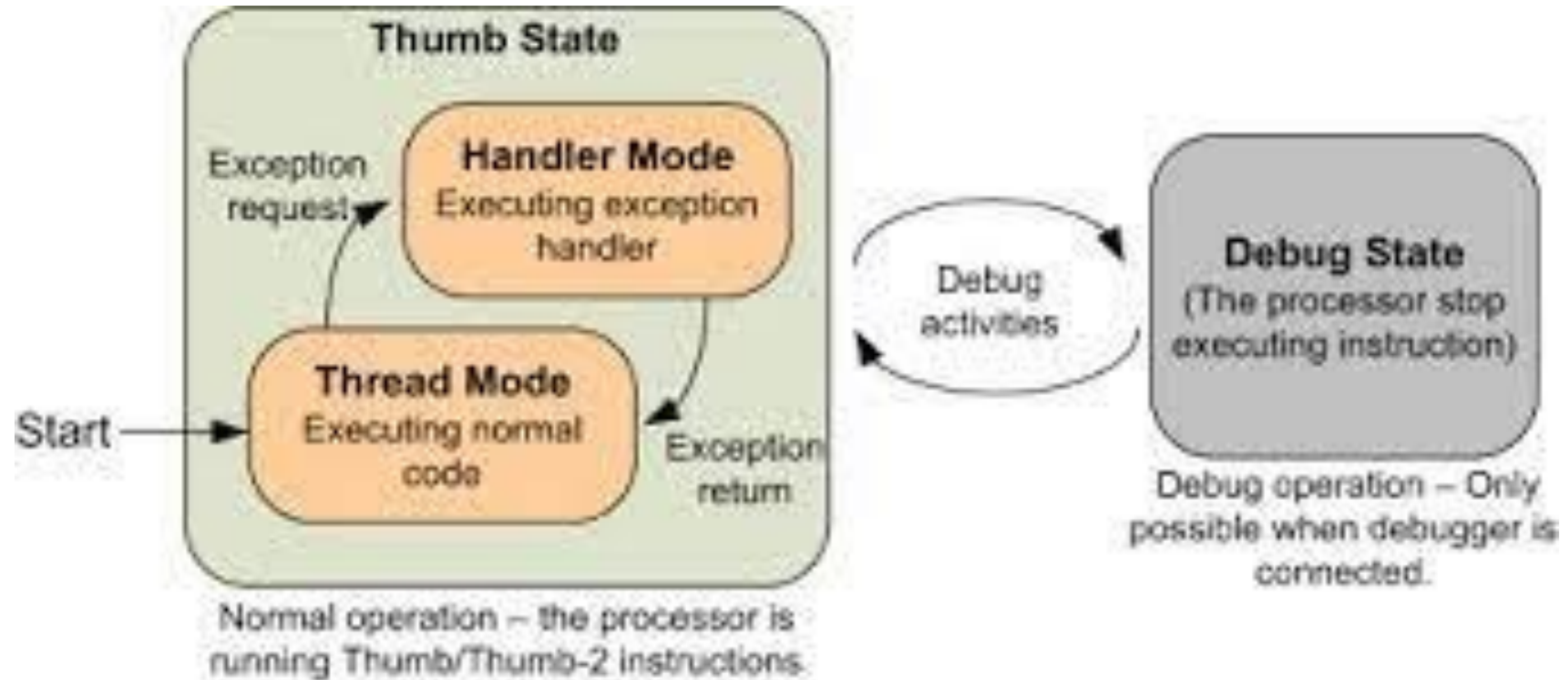
# Processor Modes - A and R



Processor mode		Description
User	usr	Normal program execution mode
FIQ	fiq	Supports a high-speed data transfer or channel process
IRQ	irq	Used for general-purpose interrupt handling
Supervisor	svc	A protected mode for the operating system
Abort	abt	Implements virtual memory and/or memory protection
Undefined	und	Supports software emulation of hardware coprocessors
System	sys	Runs privileged operating system tasks

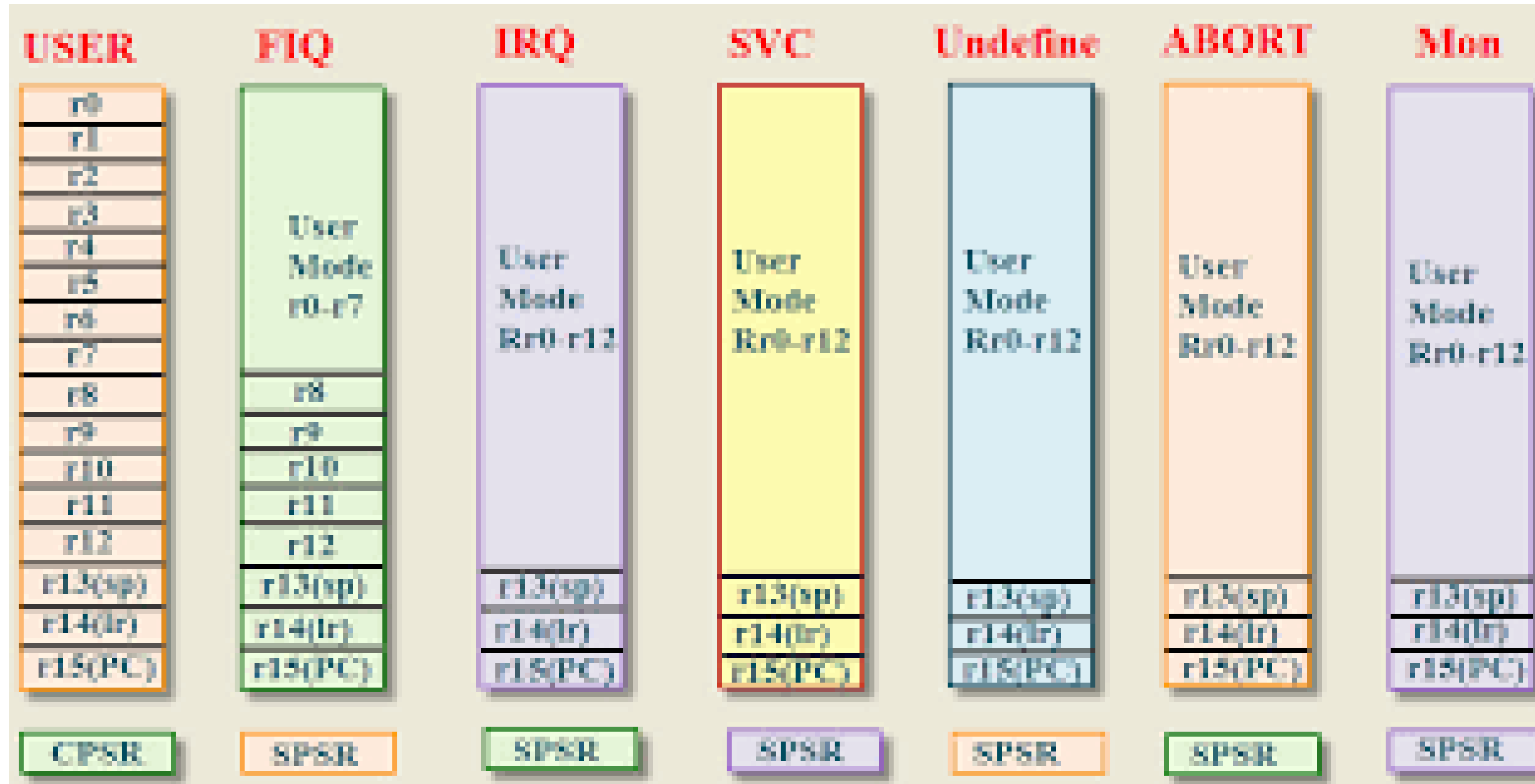


# Processor Modes – Cortex M



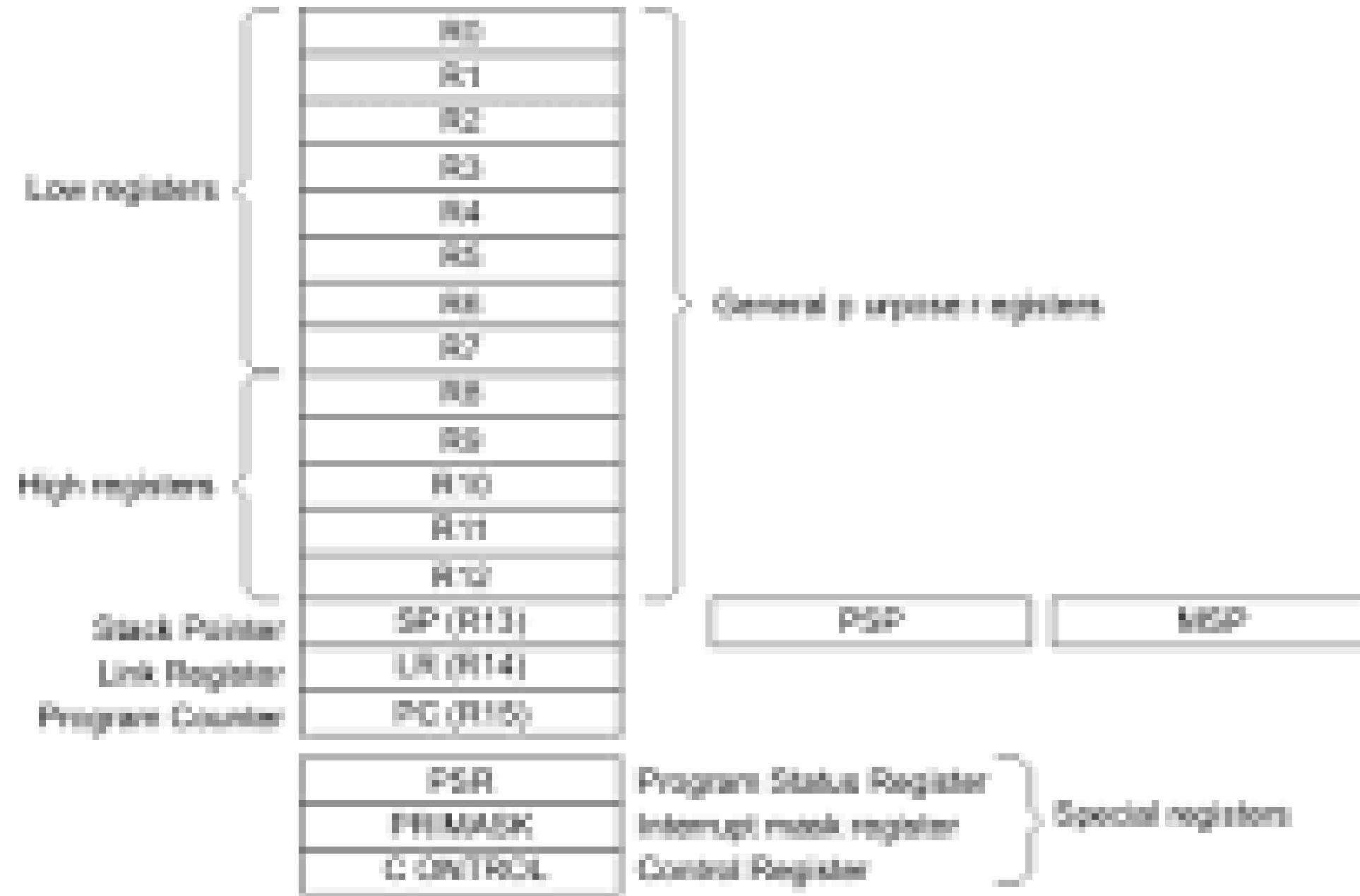


# ARM Register Set - A and R



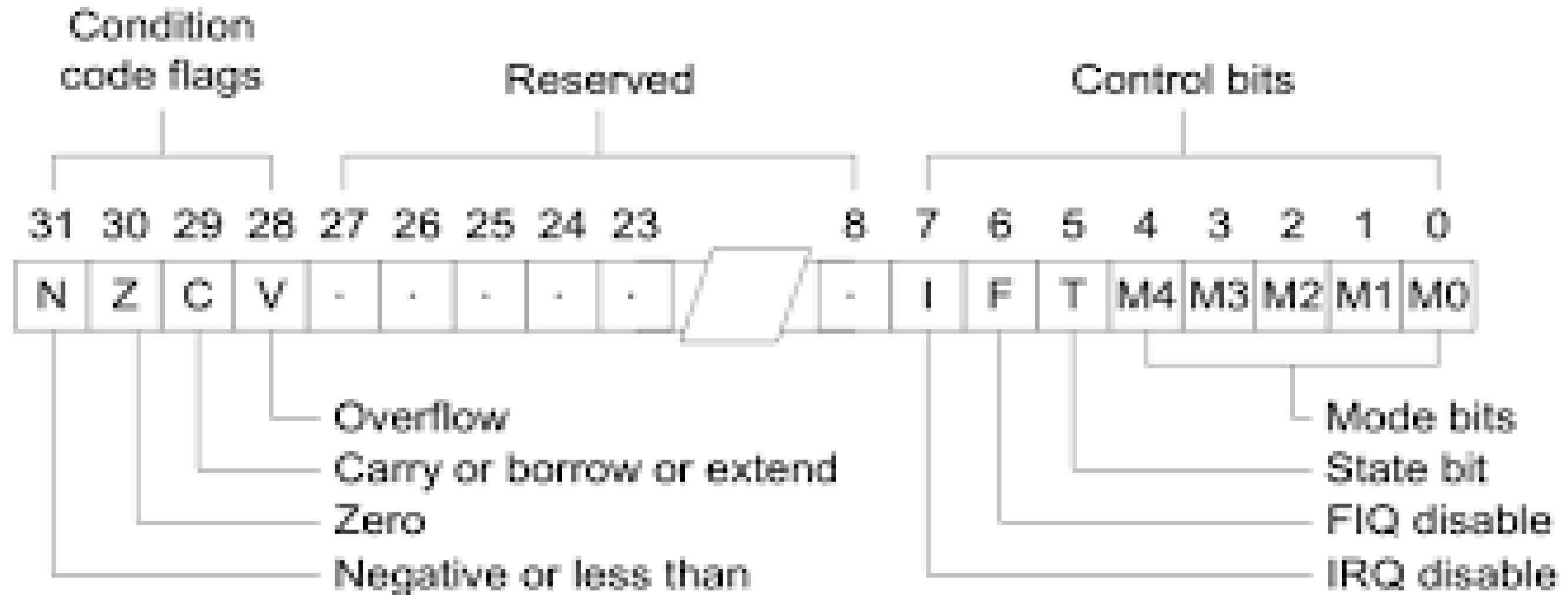


# ARM Register Set - A and R





# ARM PROGRAM STATUS REGISTER





# ARM EXCEPTIONS



Exception type	Mode	Normal address	High vector address
Reset	Supervisor	0x00000000	0xFFFF0000
Undefined instructions	Undefined	0x00000004	0xFFFF0004
Software interrupt (SWI)	Supervisor	0x00000008	0xFFFF0008
Prefetch Abort (instruction fetch memory abort)	Abort	0x0000000C	0xFFFF000C
Data Abort (data access memory abort)	Abort	0x00000010	0xFFFF0010
IRQ (interrupt)	IRQ	0x00000018	0xFFFF0018
FIQ (fast interrupt)	FIQ	0x0000001C	0xFFFF001C



# ARM Architecture



## The ARM Architecture

- Arithmetic Logic Unit
- Booth multiplier
- Barrel shifter
- Control unit
- Register file

### Arithmetic Logic Unit (ALU)

The ALU has two 32-bits inputs.

The primary comes from the register file, whereas the other comes from the shifter.  
Status registers flags modified by the ALU outputs.



# References

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*Thank You*