SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB211 – Microcontroller Programming & Interfacing

II YEAR/ IV SEMESTER

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UNIT 5 – Advanced Microcontrollers

TOPIC 3- MSP430 Functional Block Diagram

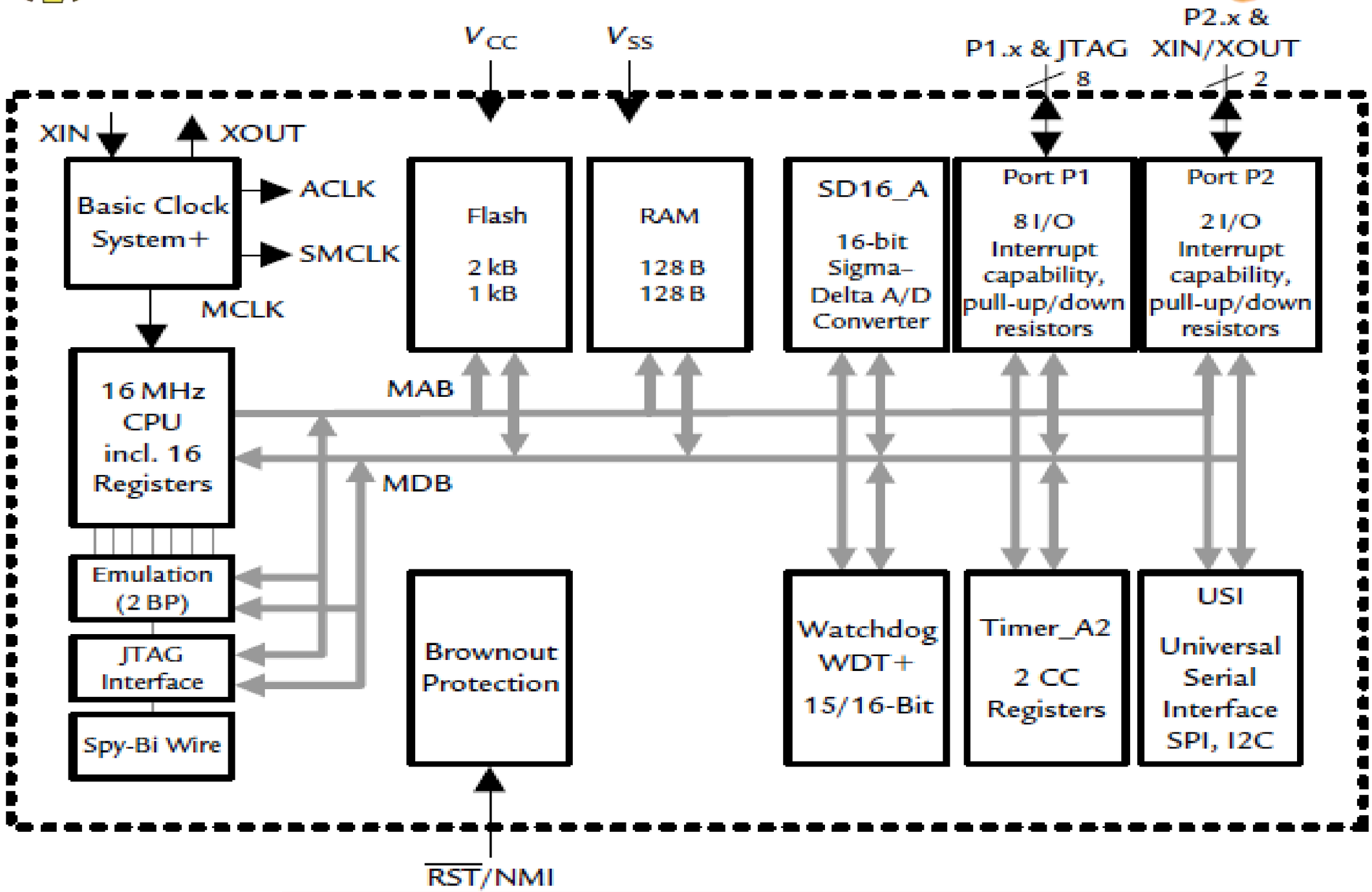
MSP430 Functional Block Diagram

- MSP430 family microcontrollers from Texas Instruments (TI), are designed for low cost, low power and portable embedded applications
- MSP430 has 16-bit RISC based processor architecture
- It supports different Low power modes
- It has 16 registers : R0-R15
- All registers are 16-bit wide
- It has 16-bit Address bus and 16-bit data bus
- Supports 27 core instructions, 24 emulated instructions and 7 addressing modes
- It is capable of wake-up time below 1 microsecond
- Extensive vectored-interrupt capability
- A wide range of on-chip peripherals are available

MSP430 Functional Block Diagram

- The main blocks are linked by the memory address bus (MAB) and memory data bus (MDB).

MSP430 Functional Block Diagram



MSP430 Functional Block Diagram

16-bit CPU

- It consists of 16-bit ALU, set of 16-registers (R0 – R15) and Logic needed to decode and execute the instructions
- The CPU has RISC architecture
- Instructions processing on either bits, bytes or words
- Supports 27 instructions and 7 addressing modes
- It can address the complete address range without paging

- CPU clock : 16 MHz
- Operating voltage : 1.8–3.6 V
- Active operation : 200 µA/MIPS
- RTC mode operation : 0.7 µA
- RAM retention : 0.1 µA
- Fast wake-up from standby mode in less than 1 µs

MSP430 Functional Block Diagram

Basic Clock system

- The clock module provides the CLK for CPU and peripherals. Three clock signals are available from the basic clock module

MCLK : Master clock is used by CPU and system
SMCLK : Subsystem Master clock is distributed to high speed peripherals
ACLK : Auxiliary clock is also distributed to low speed peripherals

The emulator and JTAG interface

The emulation, JTAG interface and Spy-Bi-Wire are used to communicate with a desktop computer when downloading a program and for debugging.

Flash memory

Flash memory is used to store the programs and constant variables
The size of Flash memory in MSP430F2003 is 1 KB
The size of Flash memory in MSP430F2003 is 2

MSP430 Functional Block Diagram

RAM

RAM is used to store the temporary data (Read/Write memory)

The size of RAM in MSP430F2003 and F2013 is 128 Bytes

16-bit Sigma Delta ADC : SD16_A

The SD16_A is ahigh performance 16-bit analog to digital converter used to interface analog signals with 200 KSPS

I/O ports : P1 & P2

The MSP430 has Two I/O ports: Port-P1 and Port-P2

The Port-P1 has 8- I/O pins and P2 has 2- I/O pins

Each I/O pin is individually configurable for input (or) output.

Each pin can be configurable for pull-up / pull-down resistors

Ports P1 and P2 have interrupt capability

MSP430 Functional Block Diagram

Watch Dog Timer

▪ A watchdog timer (WDT) is an electronic timer that is used to detect and recover from computer malfunctions. The WDT module restarts the system on occurrence of a software problem (or) if a selected time interval expires.

▪ During normal operation, the system regularly restarts the WDT to prevent it from elapsing, or "timing out". If the system fails to restart the WDT due to a hardware fault (or) program error, the timer will elapse and generate a timeout signal.

▪ The timeout signal is used to initiate corrective actions like placing the system in a safe state and restoring normal system operation.

MSP430 Functional Block Diagram

Timer_A2

- Timers are essential to almost any embedded application

- Timers are used to
- Generate fixed-period events
- Periodic wakeup - Count edges
- Generate delays - Measure time intervals
- Replacing delay loops with timer calls allows CPU to sleep, consuming less power

- Timers can support multiple capture/compares, PWM outputs, interval timing and extensive interrupt capabilities

MSP430 Functional Block Diagram

Universal Serial Interface (USI) :
The Universal Serial Interface (USI) module supports multiple serial communication modes
UART : Asynchronous, Full duplex
SPI : Serial Peripheral Interface - Synchronous, Full duplex
I2C : Serial Peripheral Interface -Synchronous, Half duplex

Brown out Reset

- The brownout protection comes into action if the supply voltage drops to a dangerous level
- The brownout reset circuit detects low supply voltages such as when a supply voltage is applied to (or) removed from the VCC terminal. The brownout reset circuit resets the device by triggering a POR (Power on Reset) signal when power is applied (or) removed. The brownout circuit is used to provide the proper internal reset signal to the device during power ON and power OFF.

MSP430 Functional Block Diagram

- The Supply Voltage Supervisor (SVS) is used to monitor the supply voltage or an external voltage. The SVS can be configured to set a flag or generate a POR reset when the supply voltage or external voltage drops below a user selected threshold.

THANK YOU