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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

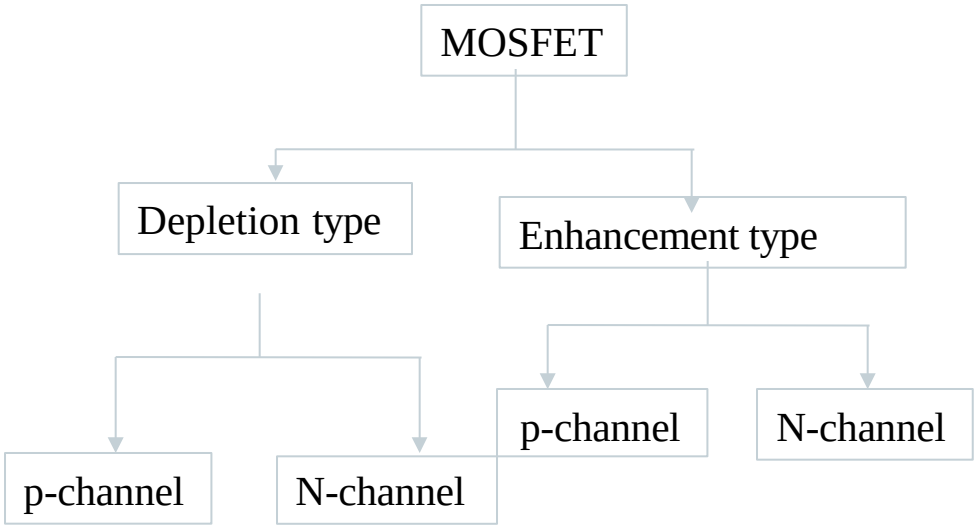
23ECB101 – CIRCUIT ANALYSIS AND DEVICES

I YEAR/ II SEMESTER

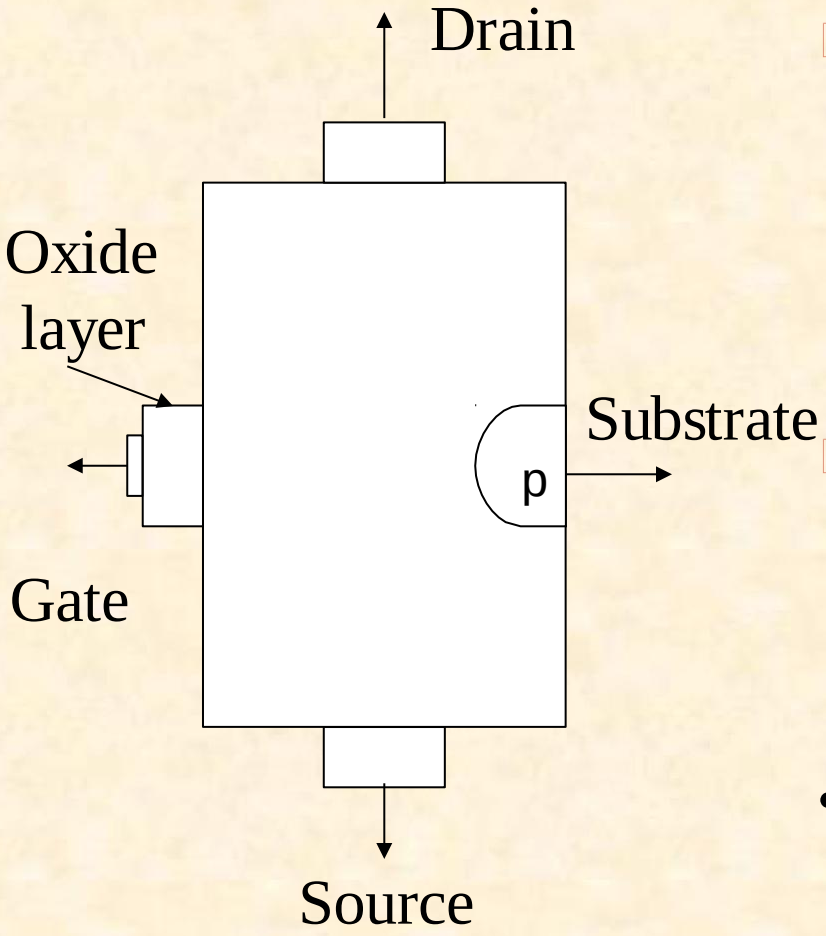
UNIT 4 – TRANSISTORS AND THEIR APPLICATIONS

TOPIC - MOSFET

Classification of MOSFETs



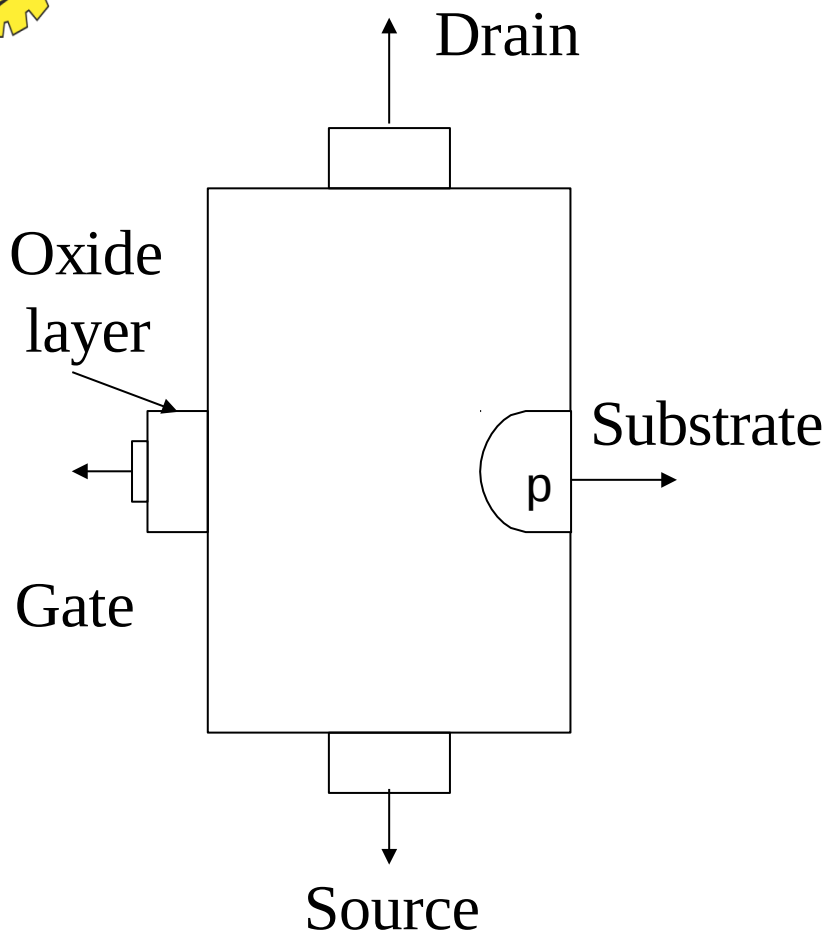
Metal oxide semiconductor field effect transistor (MOSFET)



N Channel

- MOSFET is an important semiconductor device and is widely used in many circuit application.
- The input impedance of a MOSFET is much more than that if a FET because of very small leakage current.
- MOSFETs has much greater commercial Importance than JFET

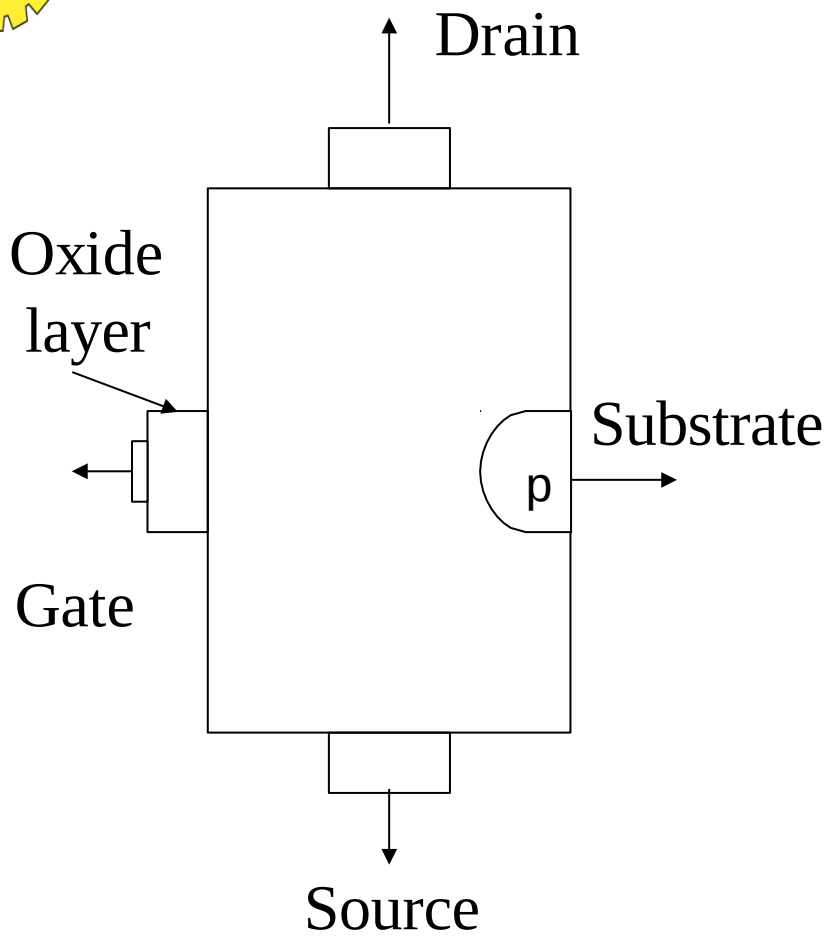
MOSFET (contd)



N Channel

- The MOSFET can be used in any of the circuits covered for the FET.
- Therefore all the equations apply equally well to the MOSFET and FET in amplifier connections.

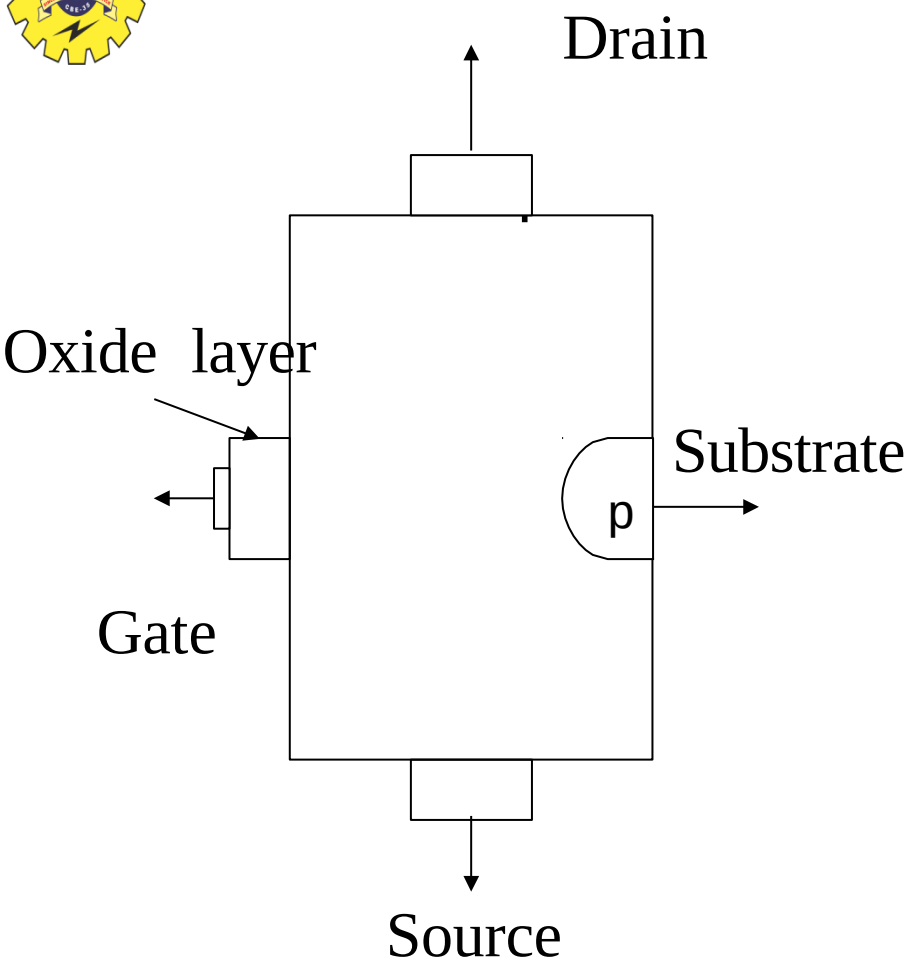
MOSFET (contd)



N Channel

- MOSFETs uses a metal gate electrode (instead of p-n junction in JFET), separated from the semi conductor by an Insulating thin layer sio_2 to modulate the resistance of the conduction channel.

MOSFET (contd)

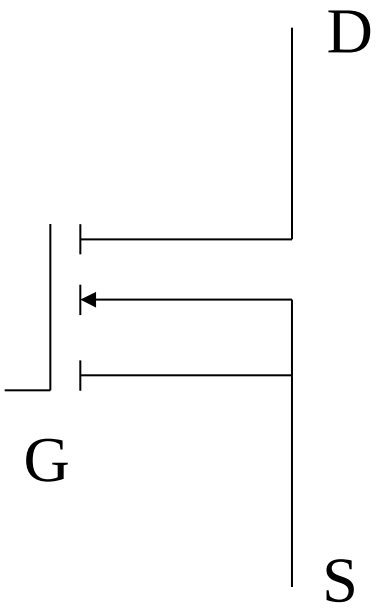


N Channel

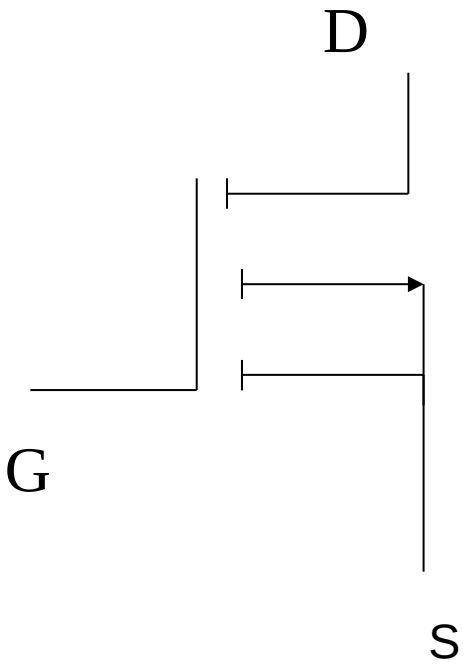
It is also called as insulated gate FET (IGFET)

MOSFETs operates both in the depletion mode as well as an the enhancement mode

CIRCUIT SYMBOLS OF MOSFET



N channel



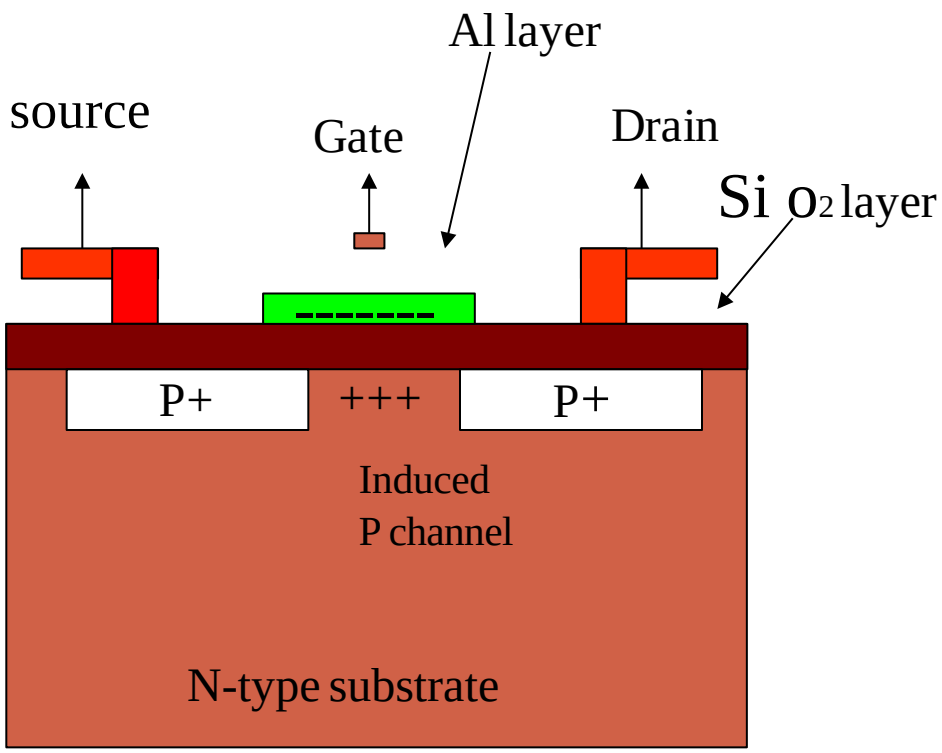
P channel

Differences between MOSFET and FET

- There is only a single *p*-region. This is called *substrate*.

- A thin layer of metal oxide is deposited over the left side of the channel. A metallic gate is deposited over the oxide layer. As silicon dioxide is an insulator, therefore a gate is insulated from the channel. For this reason MOSFET is some times called insulated gate FET.

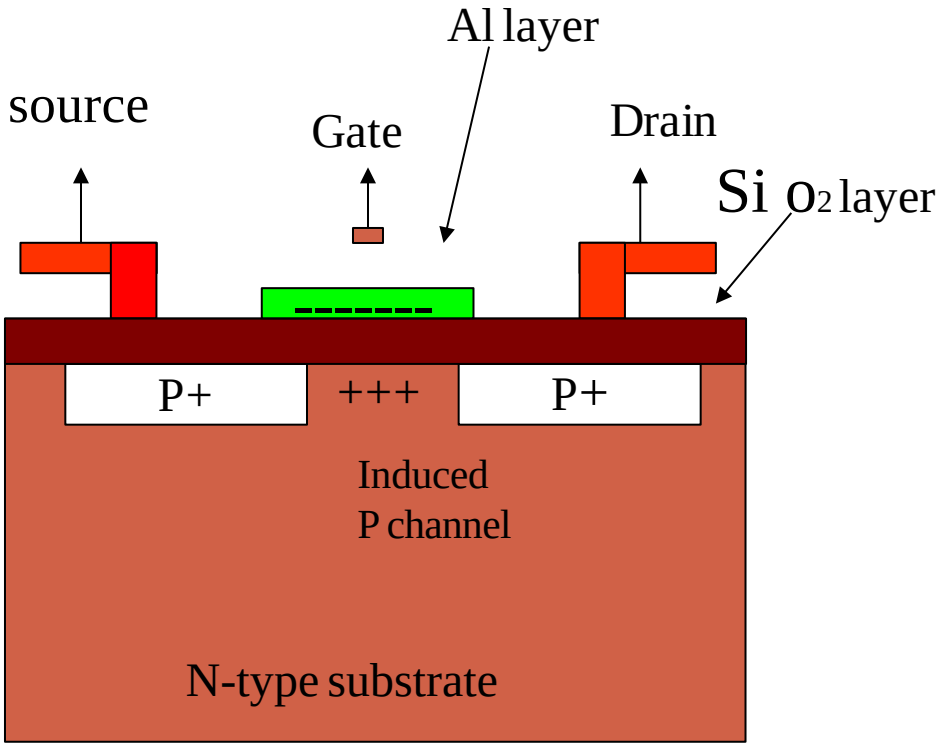
ENHANCEMENT MOSFET



- A p-channel MOSFET consists of lightly doped n-substrate into which two heavily doped p^+ regions act as the source and the drain.
- A thin layer of SiO_2 is grown over the surface of the entire assembly..

P channel Enhancement MOSFET

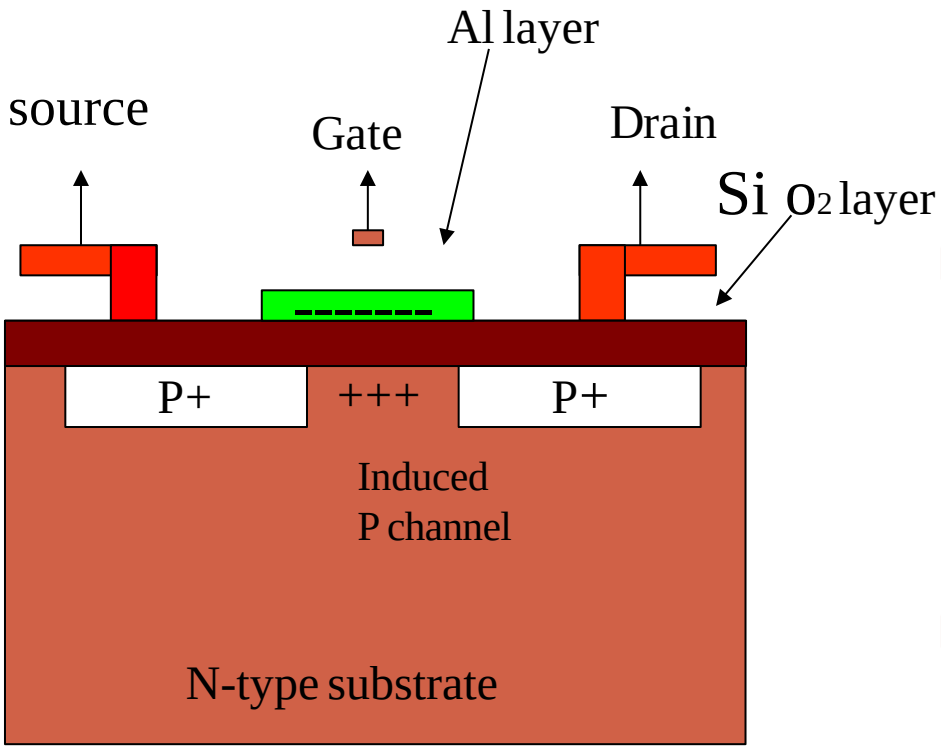
Construction



- Holes are cut into this SiO2 layer for making contact with p+ source and drain regions.
- On the S_iO_2 layer, a metal (alluminium) layer is overlaid covering the entire channel region from source to drain.
- This aluminum layer constitutes the gate.

P channel Enhancement MOSFET

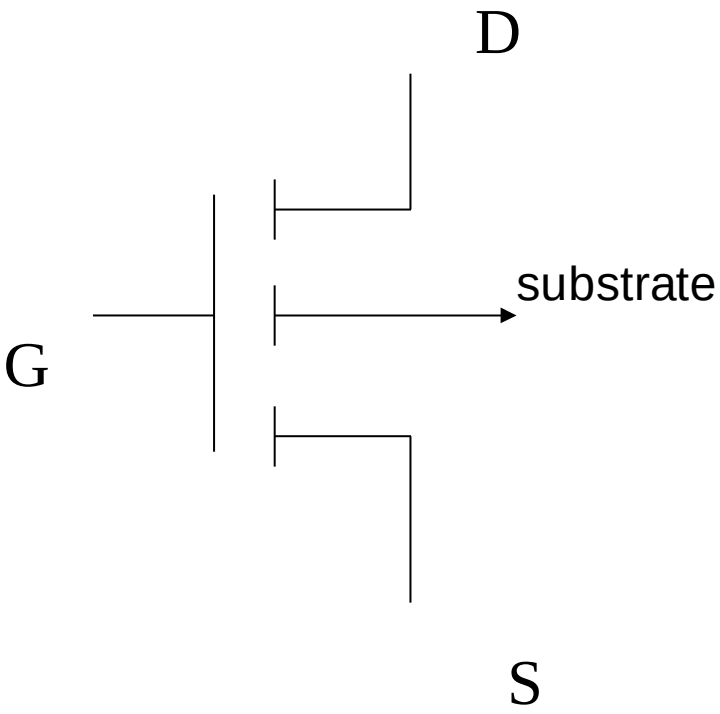
Construction



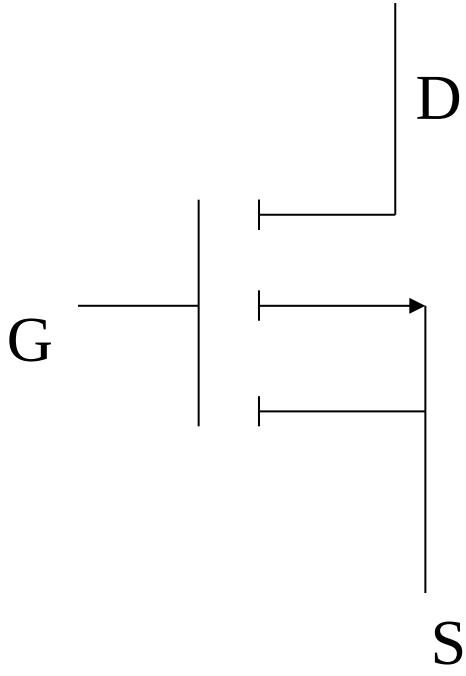
- The area of MOSFET is typically 5 square mills or less.
- This area is extremely small being only about 5% of the area required for a bipolar junction transistor.
- A parallel plate capacitor is formed with the metal areas of the gate and the semiconductor channel acting as the electrodes of the capacitor.
- The oxide layer acts as the dielectric between the electrodes.

P channel Enhancement MOSFET

symbols

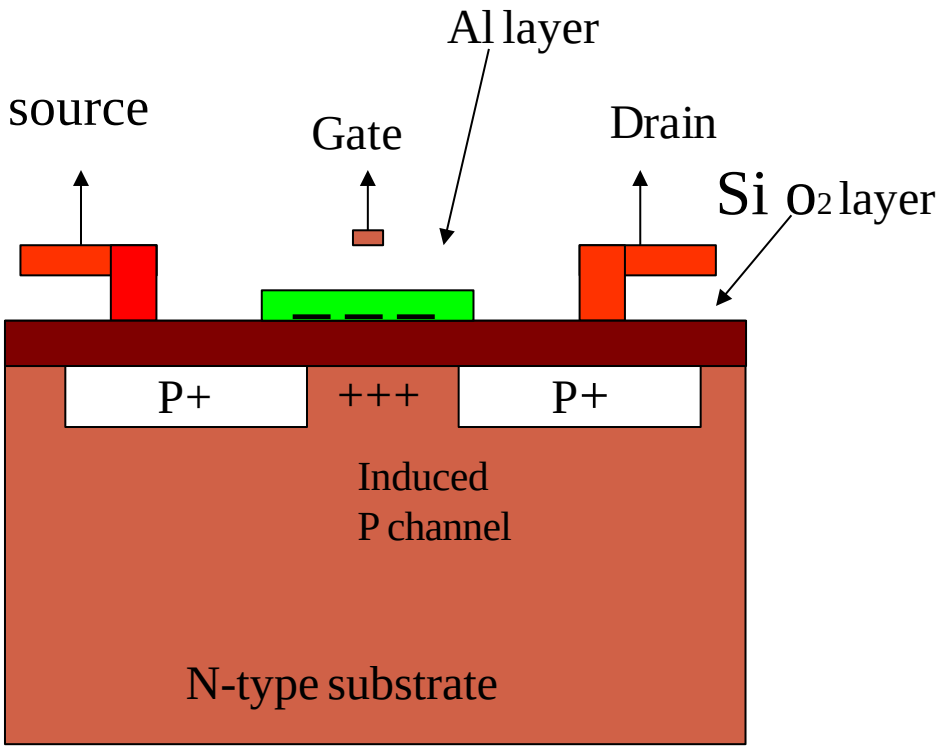


p channel enhancement MOSFET



p channel

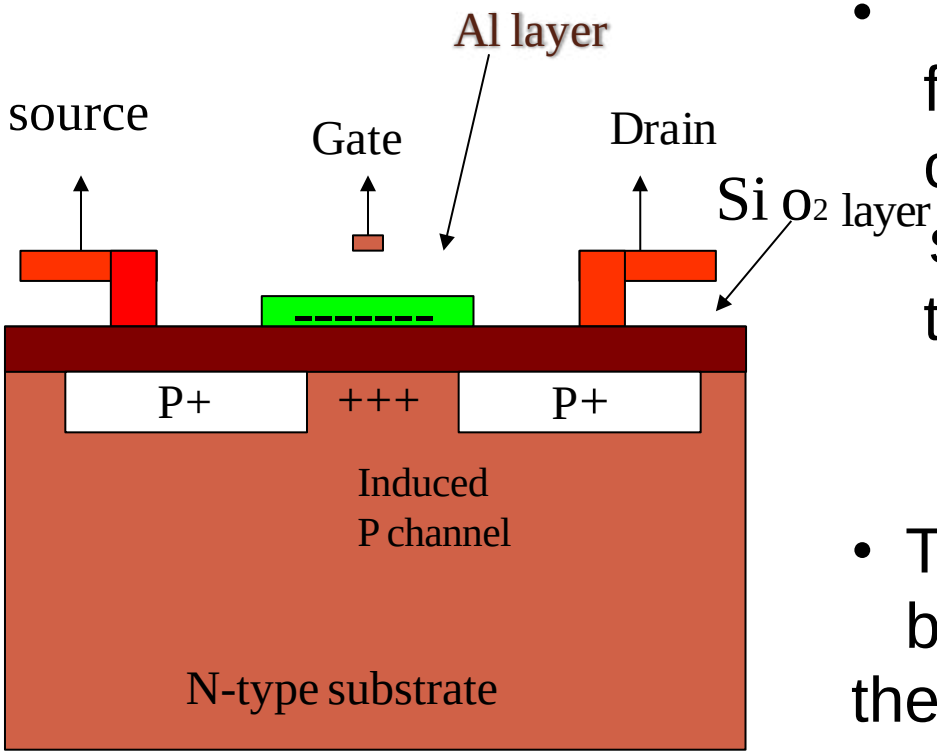
WORKING



P channel Enhancement MOSFET

- The substrate will be connected to the common terminal i.e., to the ground terminal.
- A negative potential will be applied to the gate.
- This results in the formation of an electric field normal the SiO_2 layer.

WORKING

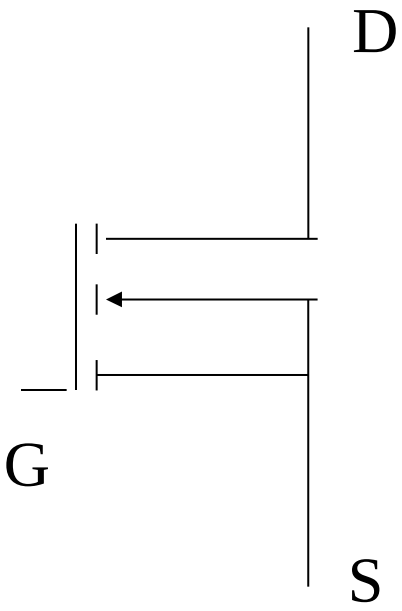


- This electric field originates from the induced positive charges on the semiconductor side on the lower surface of the SiO2 layer.

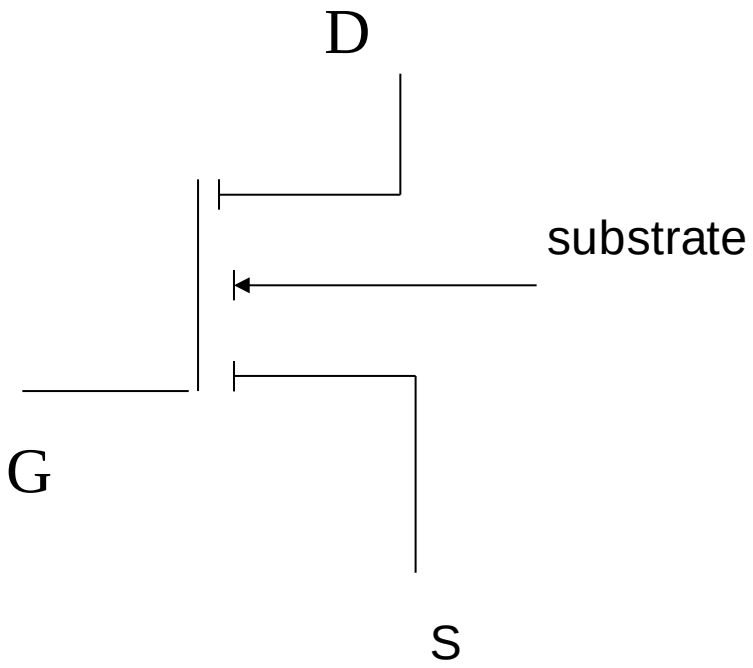
- The induced positive charge become minority carriers in the n-type of substrate.

P channel Enhancement MOSFET

Enhancement MOSFET symbols

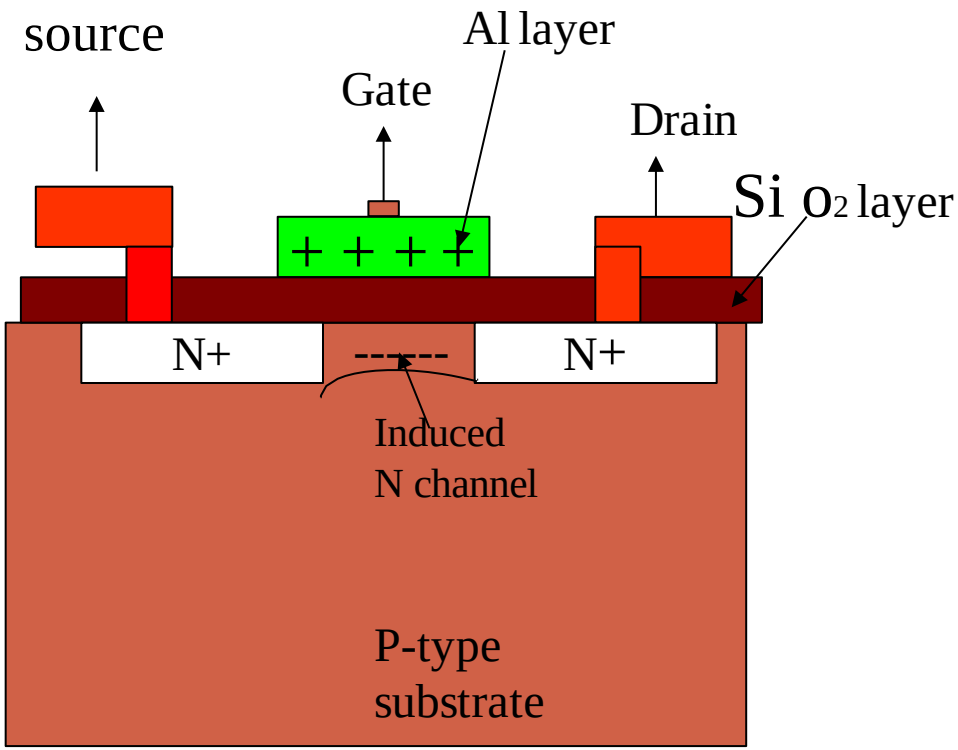


N channel



N channel

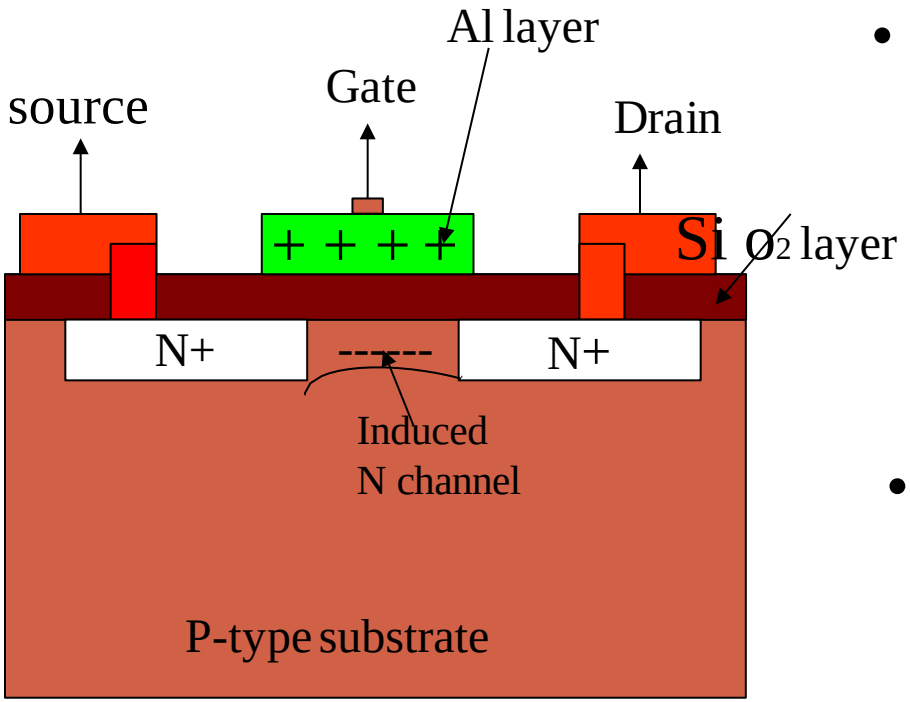
WORKING



- It consists of a lightly doped p type substrate in to which two heavily Doped n type material are diffused.
- The surface is coated with a layer of silicon dioxide(Sio_2).
- Holes are cut through the Sio_2 to make contact with n-type blocks.

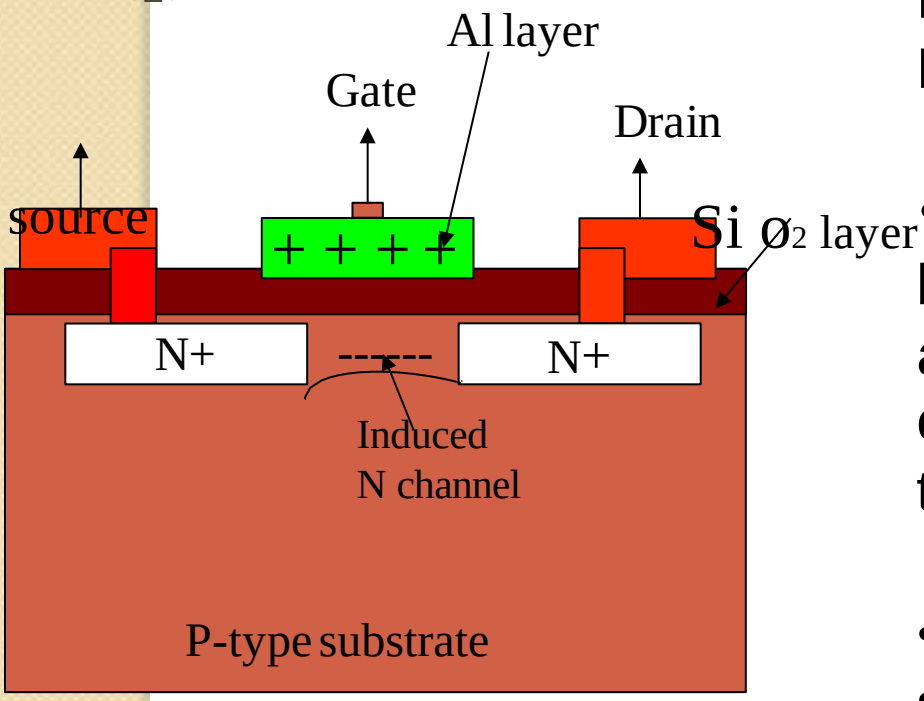
N channel Enhancement MOSFET

WORKING



N channel Enhancement MOSFET

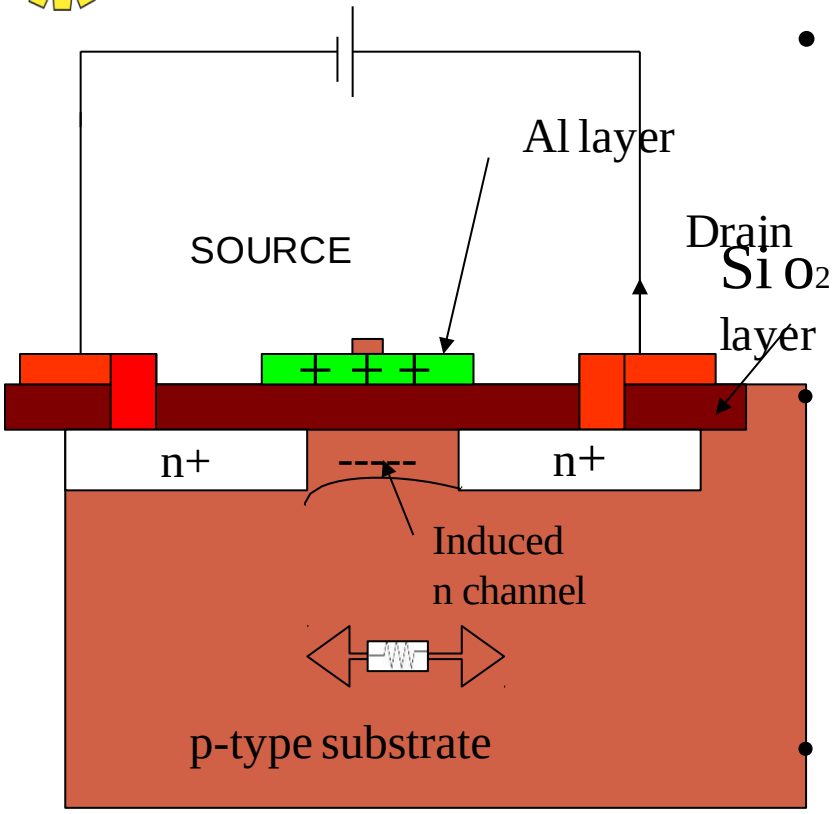
- Metal (Al) is deposited through the Holes to form drain andsource terminals
- The surface area between drain and source a metal plate is deposited from which gate terminal is taken out.



N channel Enhancement MOSFET

- Gate is insulated from the body of FET so it is called insulated gate FET(IGFET).
- Structurally there exits no channel between source and drain so MOSFET some times called as N-channel enhancement type
- Because a thin layer of P-type substrate touching the metal oxide film provides channel for electrons and hence acts like N-type material.

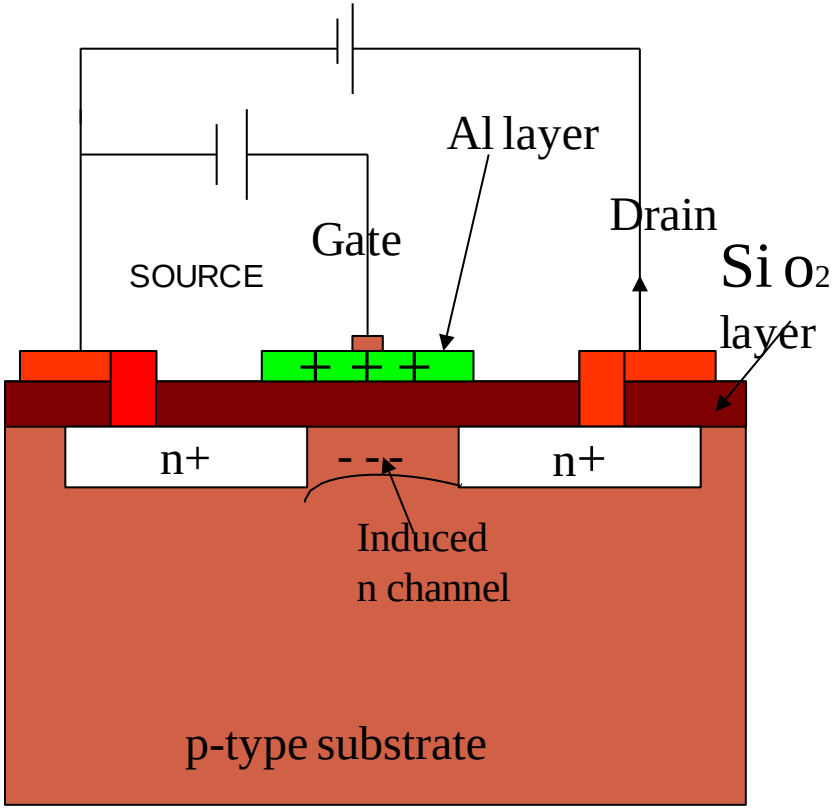
WORKING OF THE ENHANCEMENT MOSFET



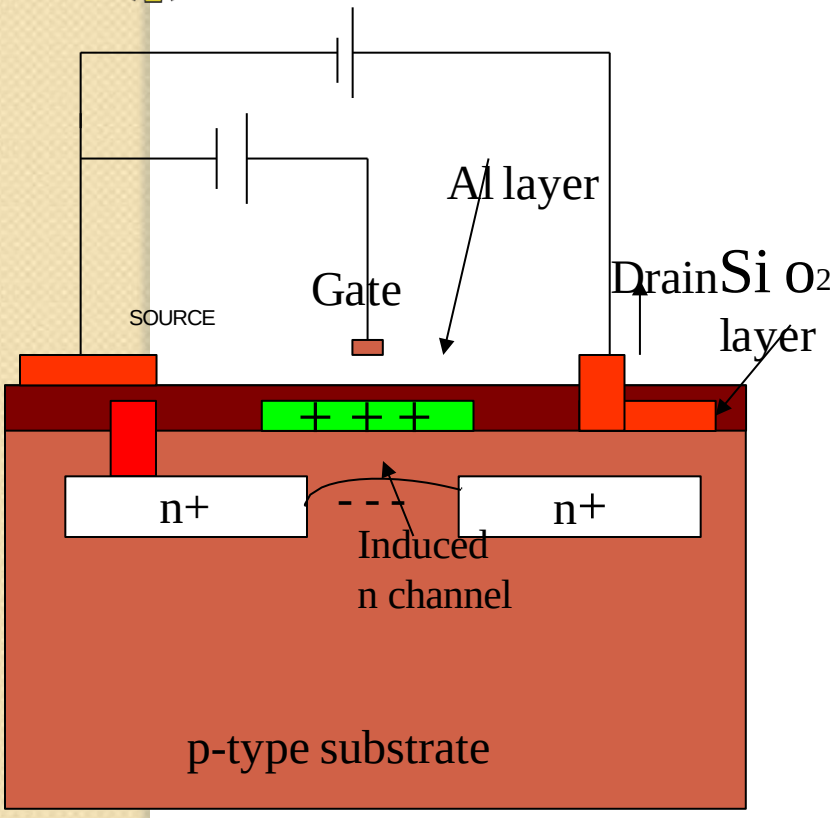
n channel Enhancement MOSFET

- Drain is made positive with respect to the source and no potential is applied to the gate as shown in figure.
- The two n-blocks and p-type substrate form back to back pn junctions connected by the Resistance of the p-type material.
- Both the junctions cannot be forwarded at the Same time so small drain current order of few nano amperes flows.

WORKING OF THE ENHANCEMENT MOSFET



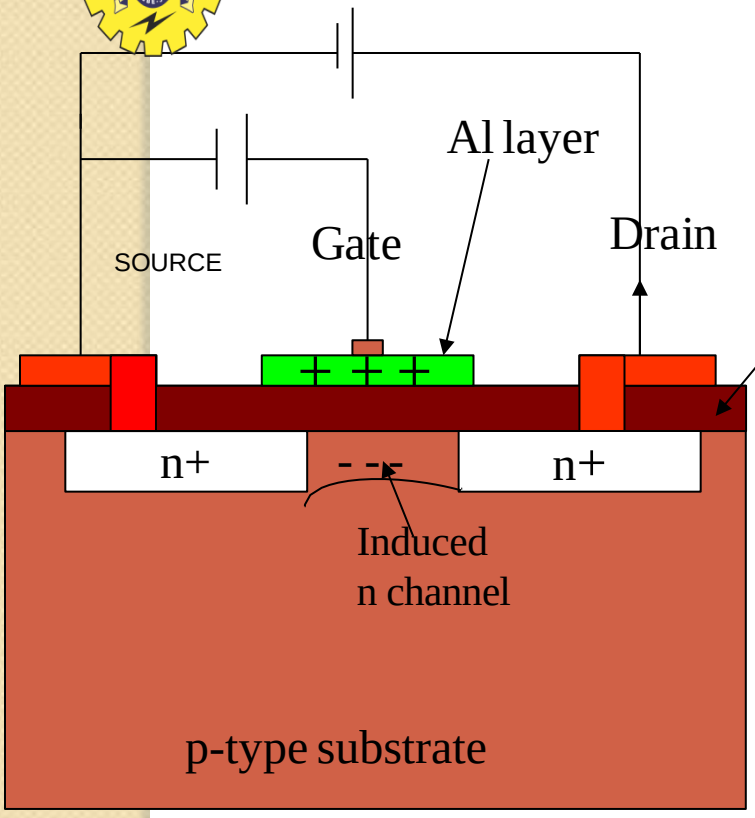
- So MOSFET is cut off when gate source voltage Is zero.
- That is why it is called normally-OFF MOSFET.
- The gate is made positive with respect to source substrate as shown in figure.
- A channel of electrons (n-channel) is formed in between the source and drain regions.



N channel Enhancement MOSFET

- Behaves as a capacitor with gate metal acting as one electrode, upper surface of the substrate as other electrode and sio2 layer as dielectric medium.

- When positive voltage is applied to gate the capacitor begin to charge.



N channel Enhancement MOSFET

- Consequently positive charges appears on the gate and negative charges appears in the substrate between the drain and source.

- The n-channel thus formed is called induced n-channel or n-type inversion layer.
  - As $V_{GS}\uparrow$,no.electrons in the channel , $I_D\uparrow$.

- The minimum gate source voltage which produces the induced n-channel is called threshold voltage $V_{GS}(th)$ when $V_{GS} < V_{GS}(th)$, $I_D = 0$.

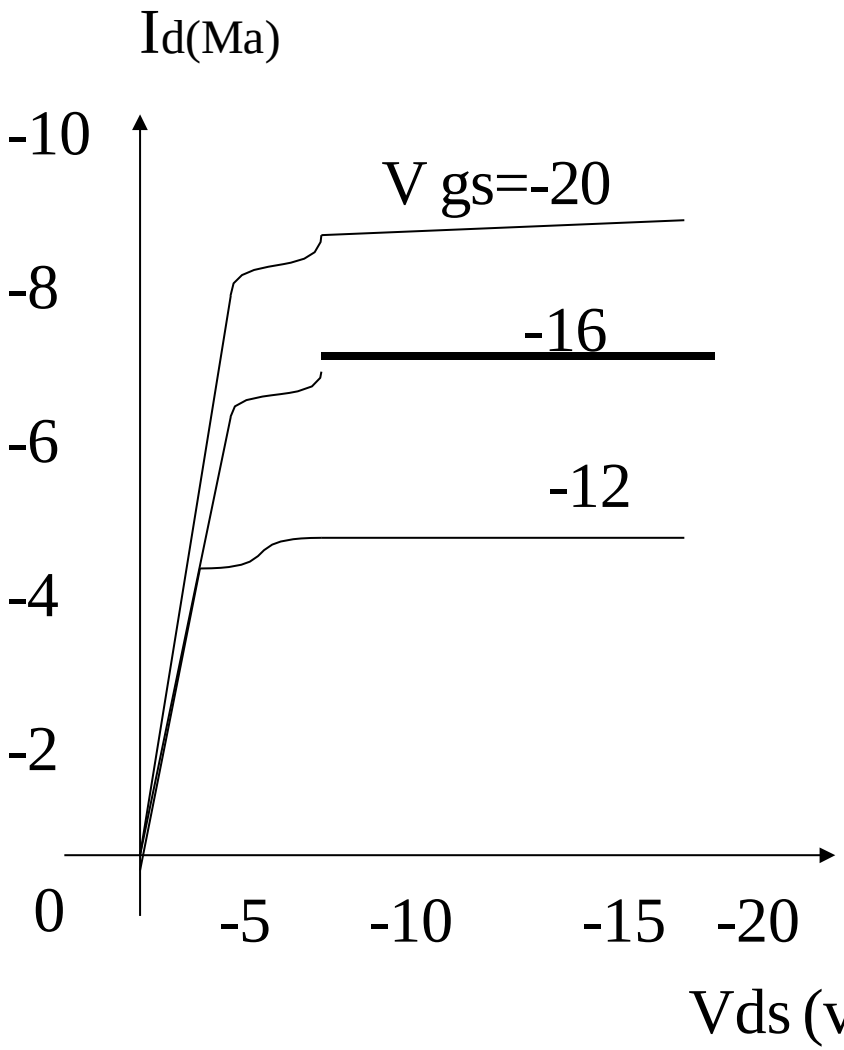
- Drain current starts only $V_{GS} > V_{GS}(th)$.

- For a given value of V_{DS} as V_{GS} is increased , more and more electrons accumulate under the gate and I_D increases.

- So the conductivity of the channel is enhanced by the positive bias on the gate, the device is known as enhancement mode MOSFET.

- The n-channel MOSFET can never operate with a negative gate voltage.

- Drain characteristics



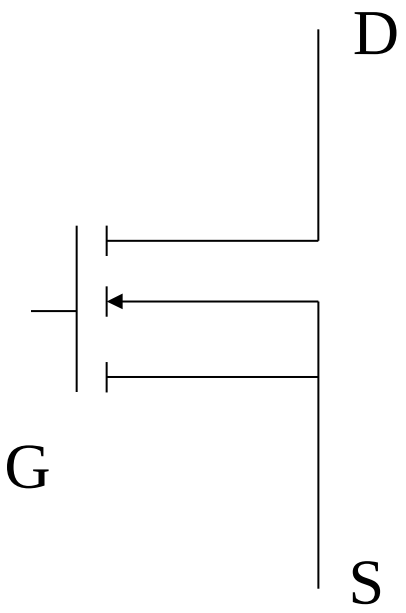
•It is observed that the drain current has been enhanced on application of negative gate voltage.

•This is the reason for calling it as enhancement MOSFET.

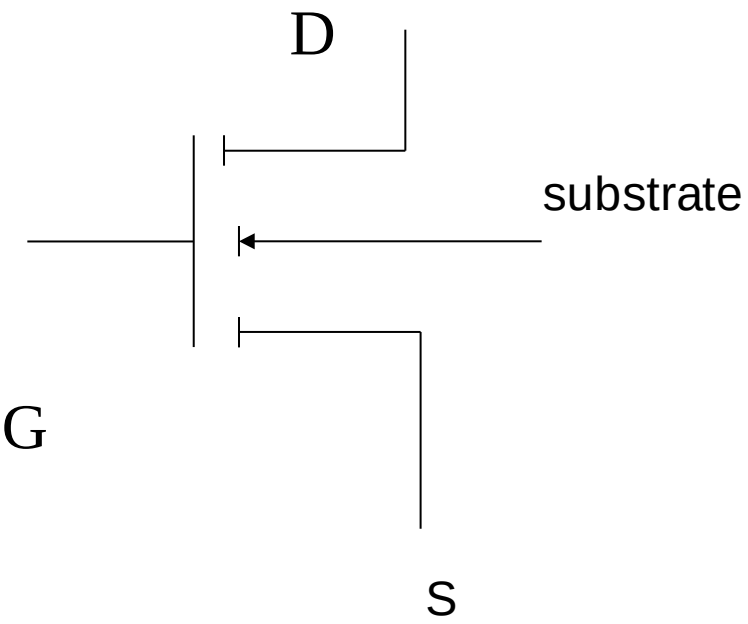
•By increasing the gate potential, pinch off voltage and drain currents are increased.

•The curves are similar to drain characteristics of JFET.

ENHANCEMENT MOSFET



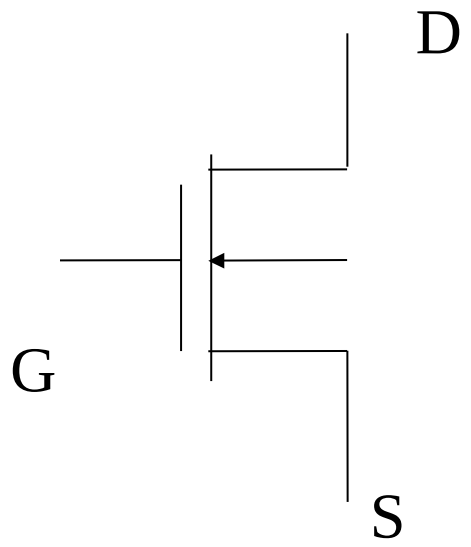
N channel



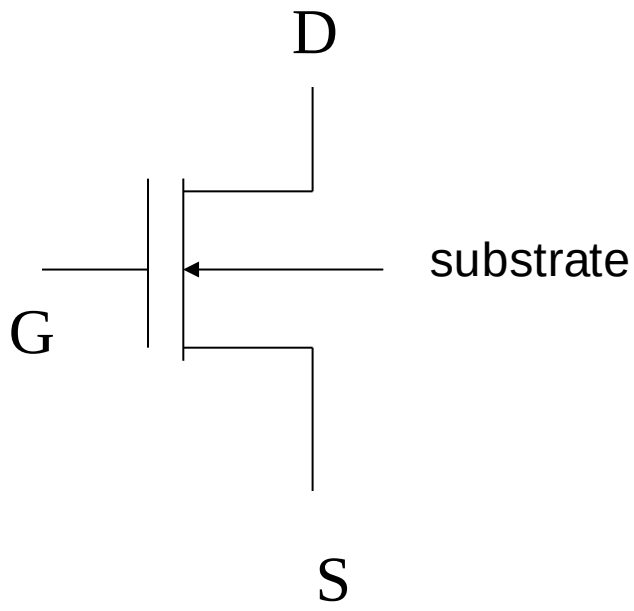
N channel

CIRCUIT SYMBOLS OF DEPLETION TYPE MOSFET

DEPLETION MOSFET

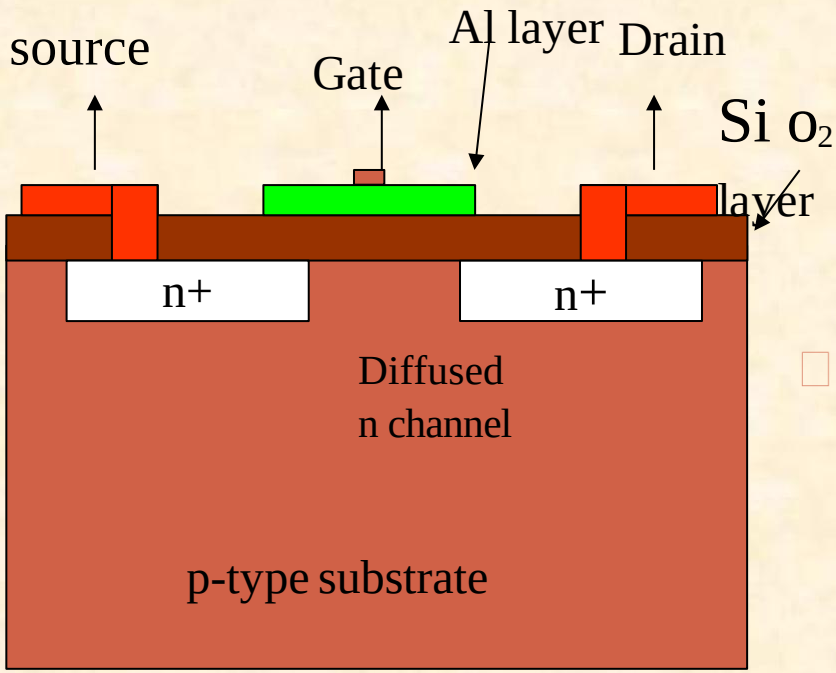


N channel



N channel

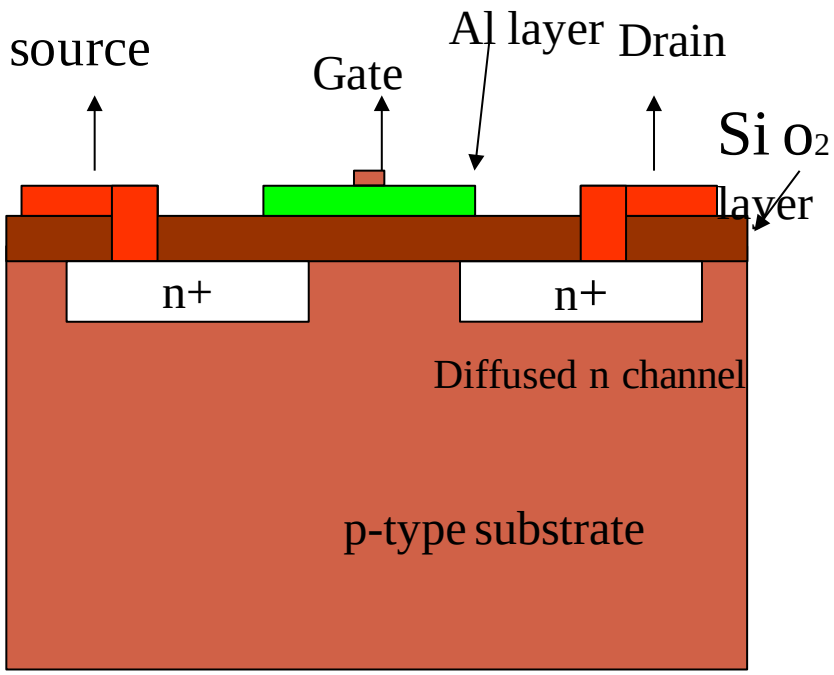
CONSTRUCTION



N channel Depletion MOSFET

- Depletion MOSFET may be fabricated from the basic MOSFET structure.
- An n-type channel is obtained by diffusion between N^+ type source and drain in an n-channel MOSFET.

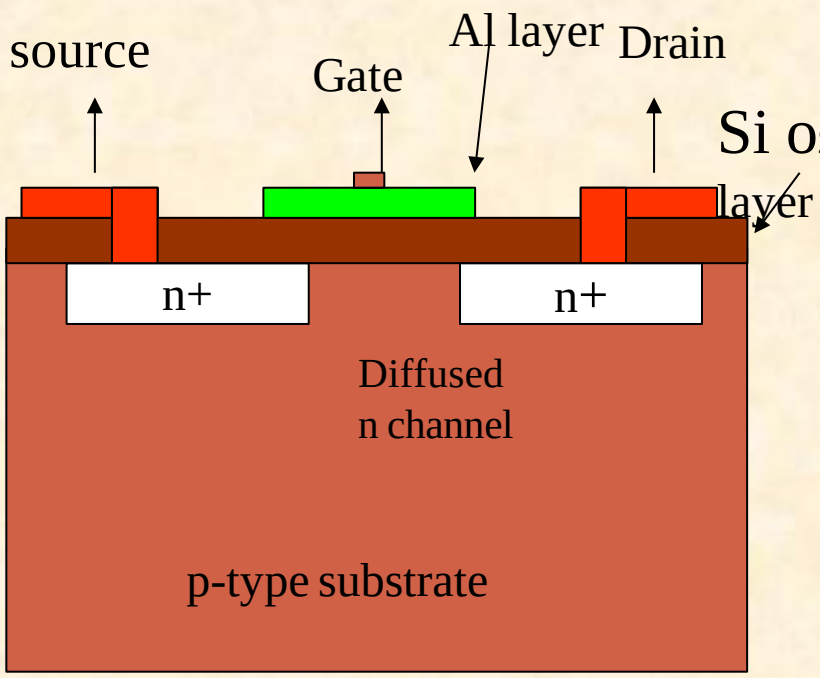
CONSTRUCTION



N channel Depletion MOSFET

- In depletion MOSFET a lightly doped n-type channel has been introduced between to heavily doped source& drain blocks,.

CONSTRUCTION OF P CHANNEL DEPLETION MOSFET



P channel Depletion MOSFET

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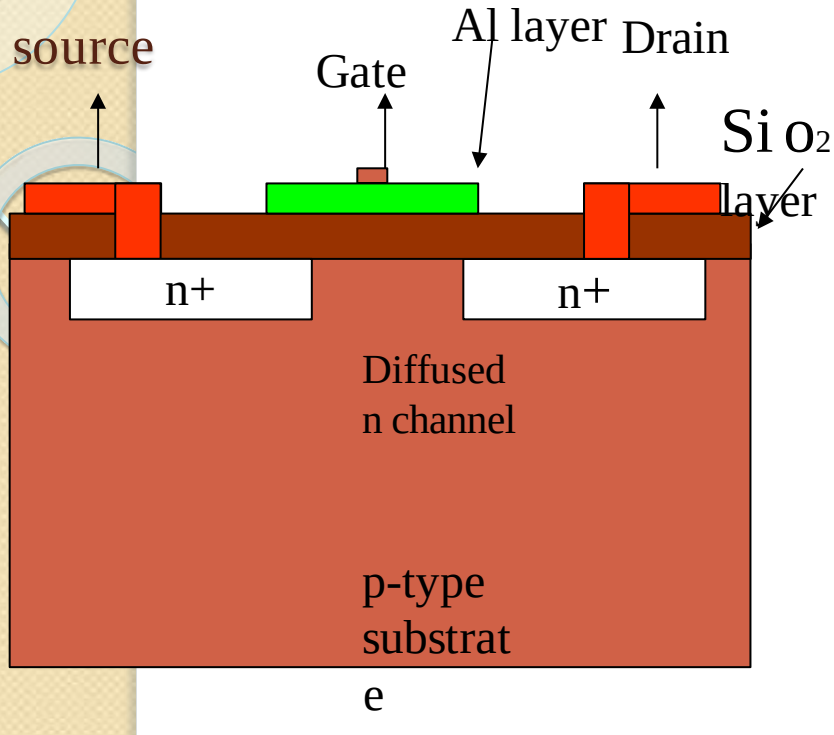
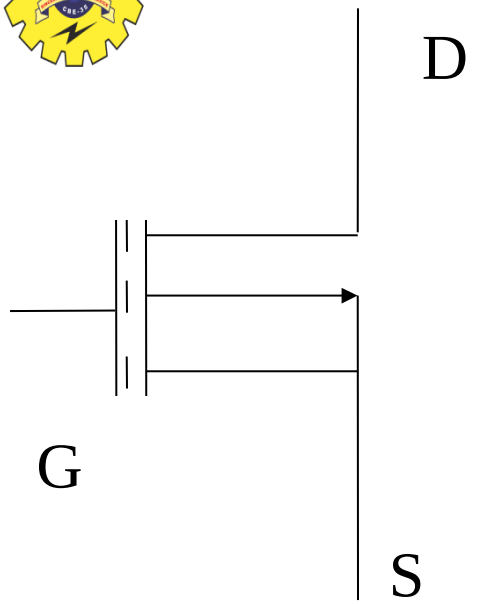


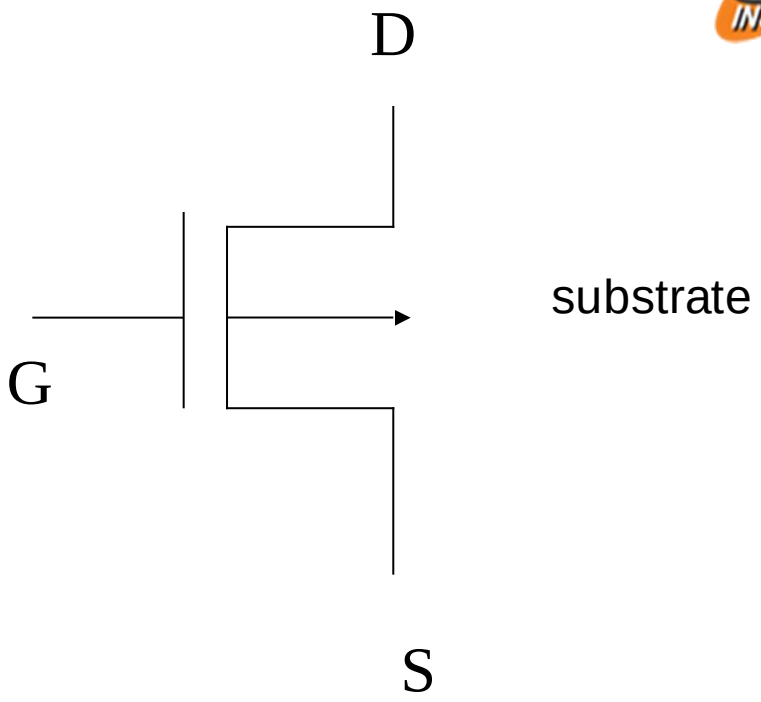
P channel Depletion MOSFET

- In p-channel depletion MOSFETs are made by using n-type substrate and diffusing a lightly doped p-type channel between two heavily doped P-type source & drain blocks

Symbols of p channel depletion MOSFET

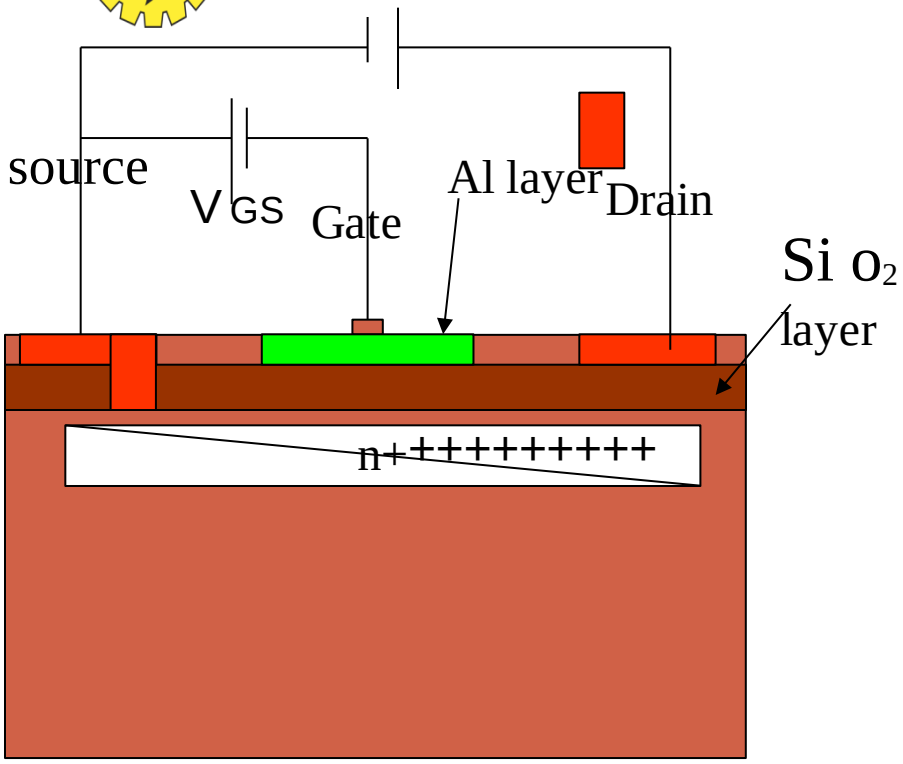


P channel



P channel

Working



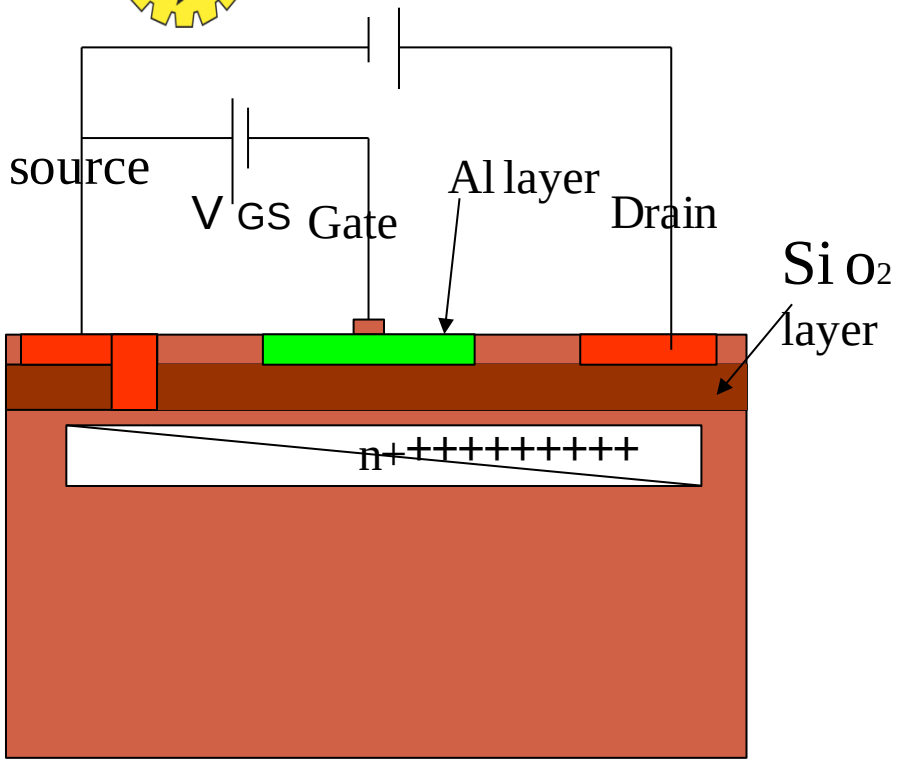
N channel Depletion MOSFET

- Negative gate operation of a depletion MOSFET is called Its depletion mode Operation

- When Vgs =0 electrons can flow freely from source to drain through the conducting channel. since a channel exists between drain & source, Id flows even when Vgs =0.

- It is also known as normally – ON MOSFET

Working

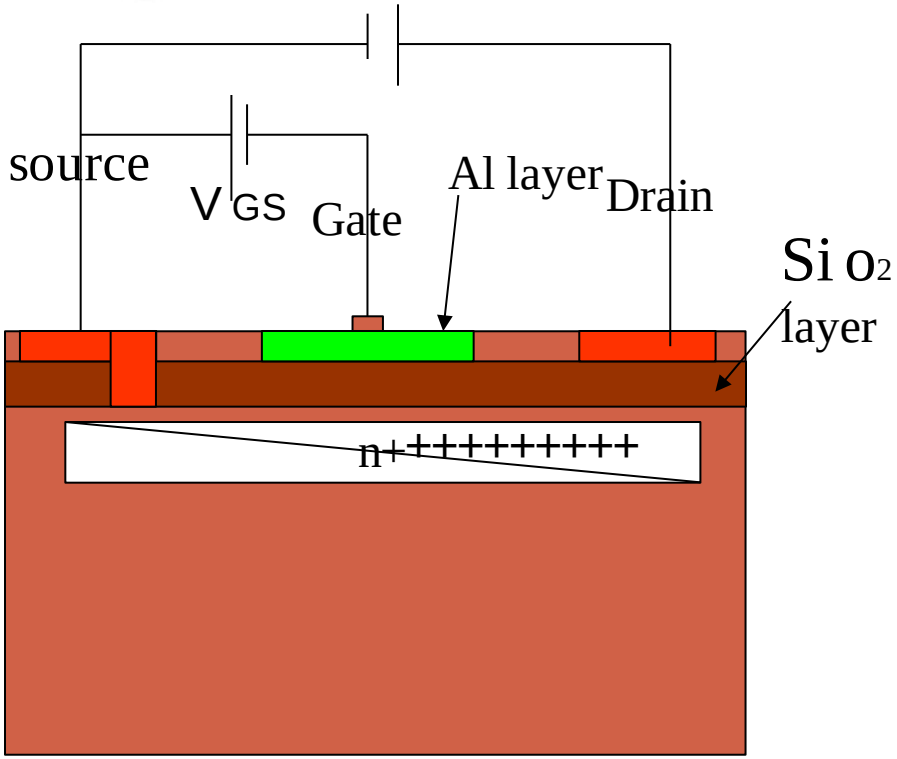


When negative voltage is applied to the gate as shown in Fig positive charges are induced in the channel by capacitor action

The induced positive charges make the channel less conductive and drain current decreases as V_{GS} is made more negative.

N channel Depletion MOSFET

Working



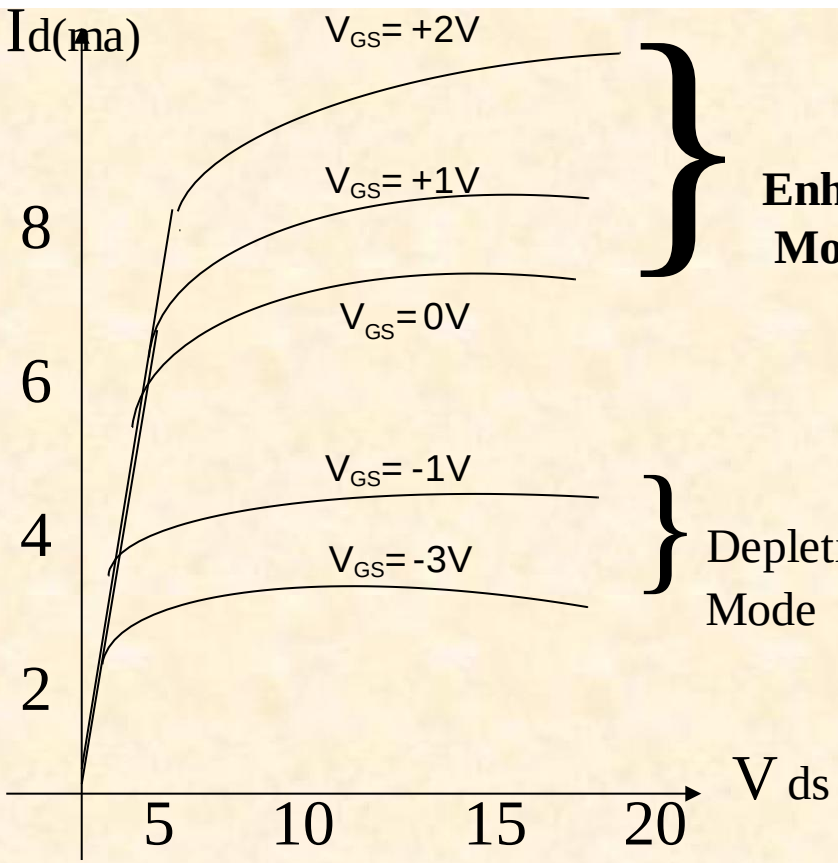
N channel Depletion MOSFET

With negative voltage a depletion MOSFET behave like JFET.

- n positive voltage is applied to the gate free electrons are Induced channel .

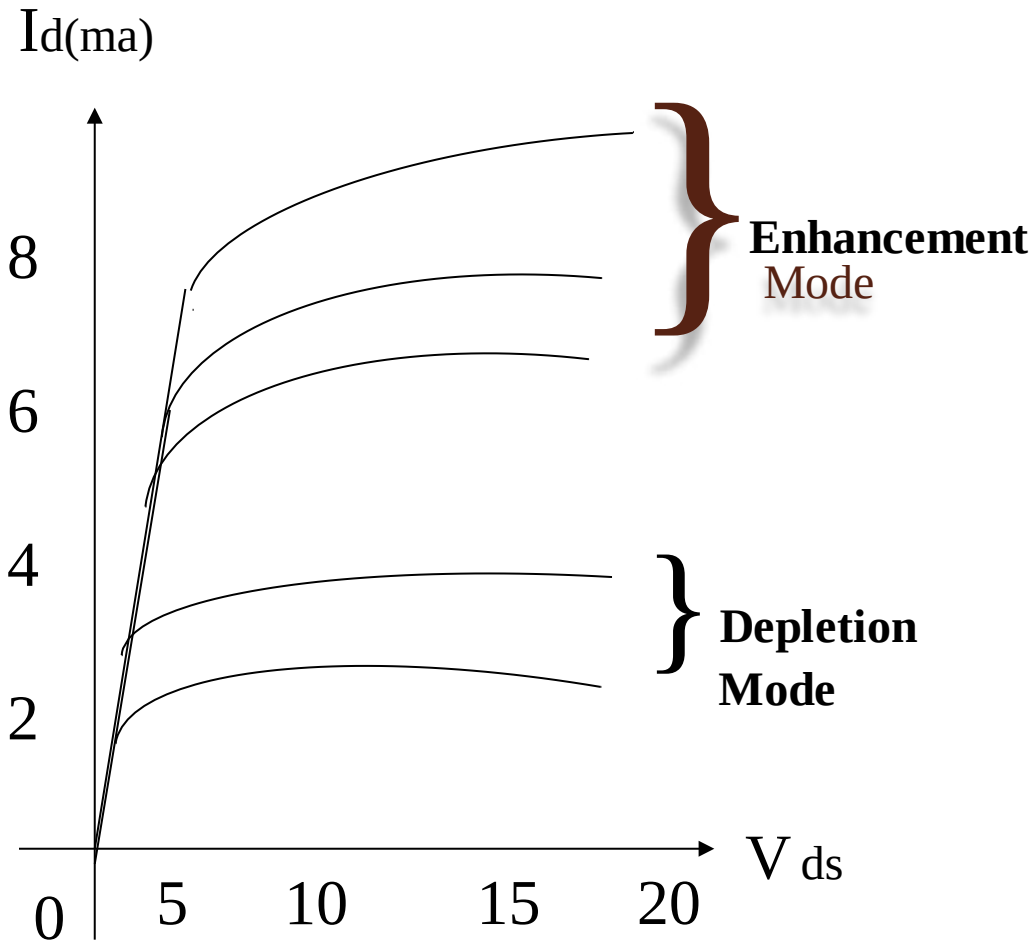
- This enhances the conductivity of the channel so increasing amount of current between terminals
- Since the action of negative voltage on gate is to deplete the channel of free n-type charge carriers so named as depletion MOSFET.

Drain Characteristics of depletion MOSFET



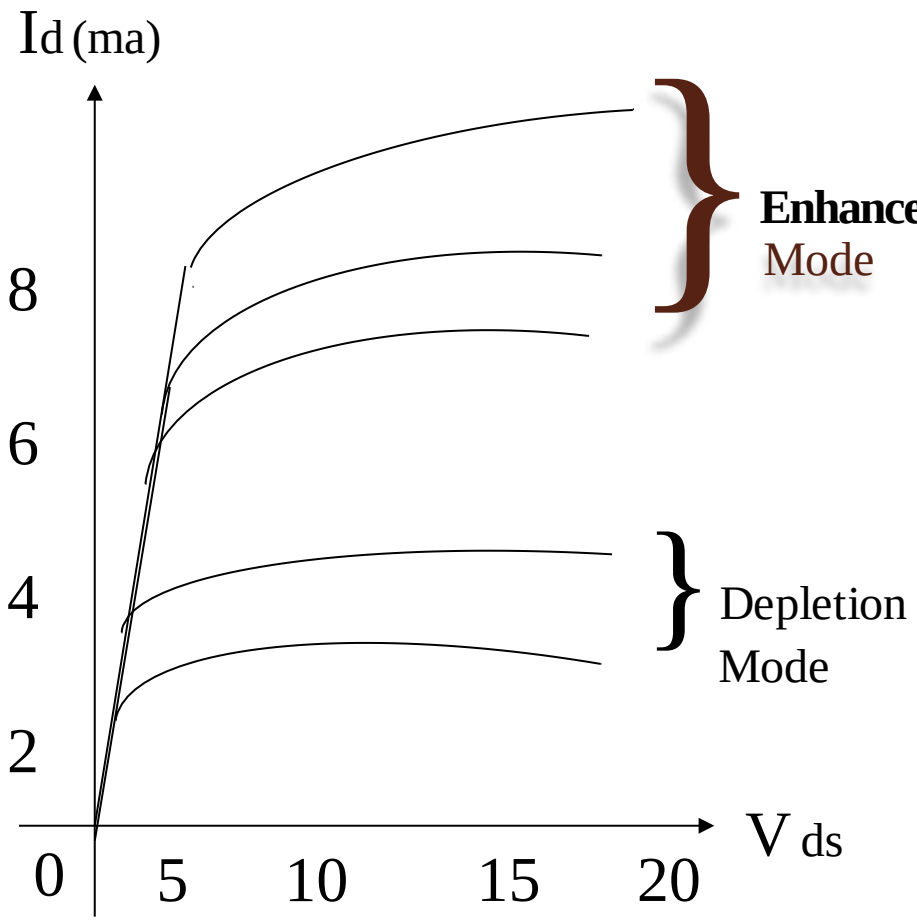
- When the gate source voltage is zero considerable drain current flows.
- When the gate is applied with negative voltage, positive charge are induced in the n-channel through the SiO_2 layer of the gate capacitor.

Drain Characteristicsof depletion MOSFET



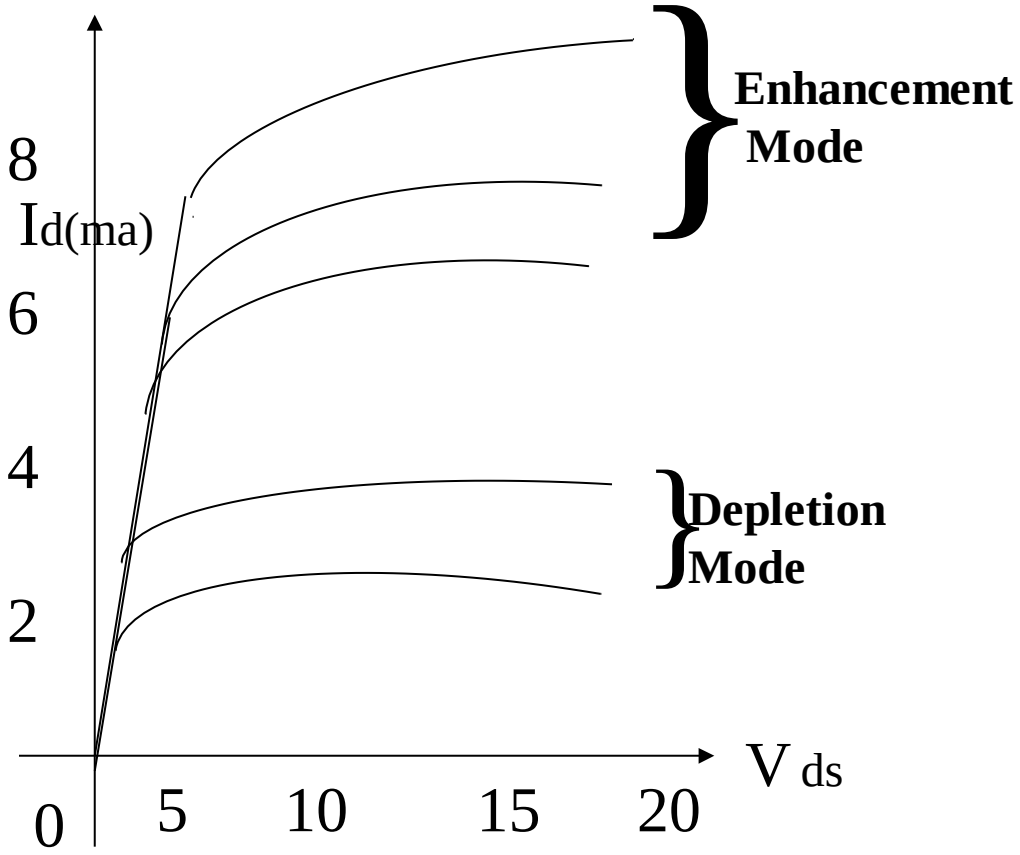
- The conduction in n-channel FET is due to electrons i.e., the majority carriers.
- Therefore the induced positive charges make the n-channel less conductive.
- The drain current therefore gets reduced with increase in the gate bias voltage.

Drain Characteristics of depletion MOSFET



- The distribution of charges in the channel results in depletion of majority carriers.
- That is why this type of FET is called depletion MOSFET.
- The voltage drop due to the drain current causes the channel region nearer to the drain to be more depleted than the region due to the source.

Drain Characteristics of depletion MOSFET



- This is similar to the pinch off in JFET.

Drain Characteristics of depletion MOSFET

- The depletion MOSFET can also be operated in enhancement mode simply by applying a positive voltage to the gate

- Application of positive gate voltage results in induced negative channel in the n-type channel

Drain Characteristics of depletion MOSFET

Thus the conductivity of the channel gets increased the n-channel depletion MOSFET can be used as in enhancement mode by changing the gate voltage polarity.

- When a MOSFET is operated this way, we can it as dual mode MOSFET.

Comparison of MOSFET and JFET

Sno	JFET	MOSFET
1.	JFET Gate is not insulated from the channel	MOSFET or IGFET is insulated from the channel
2.	Channel and gate forms two pn junctions	Channel and gate forms parrallel plate capacitor.
3.	There are only 3 leads	There are 4 leads
4.	Can be operated in depletion mode only	Can be operated inboth depletion and enhancement mode
5.	Input impedance is high	Input impedance is very high
6.	Signal handling capacity is less	Signal handling capacity is more
7.	Gate current is more	Gate current is very less Easy to
8.	Fabrication is complex and costly	fabricate,cheap. Most

Advantages of MOSFET Over JFET

- The insulated gate in MOSFET s result in much greater input impedance than that of JFET
- Inter electrode capacitance are independent of bia voltage and these capacitances are smaller incase of MOSFETs than JEFT.
- It is easier to fabricate MOSFET than JFET.
- MOSFET has no gate diode. This makes it possible to operate with +ve or –ve gate voltages

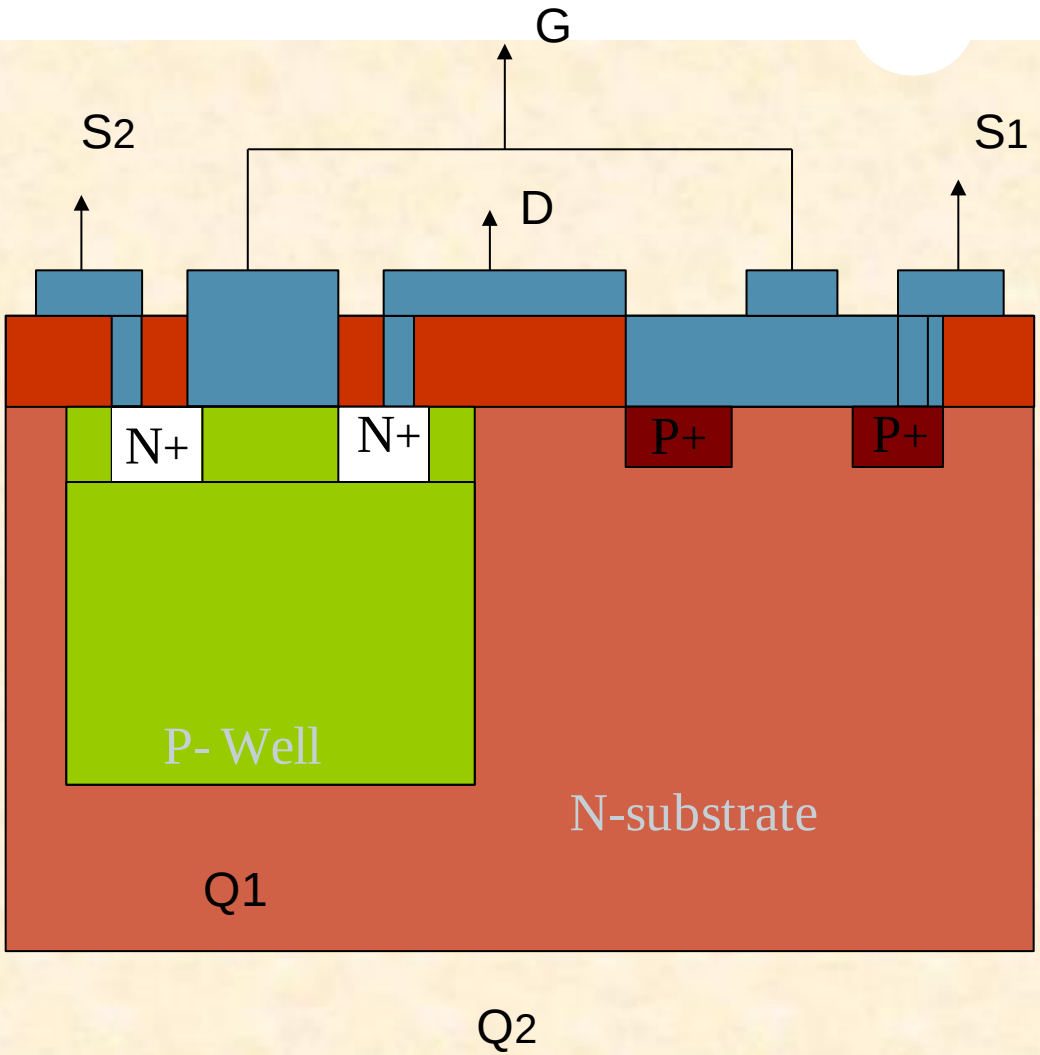
Application of MOSFETs

- Because of higher input resistance ,the enhancement type MOS devices have been used as micro-resistor in integrated micro-circuits .

- For electrometer circuits where exceptionally low currents are to be measured MOSFETs are most nearly ideal.

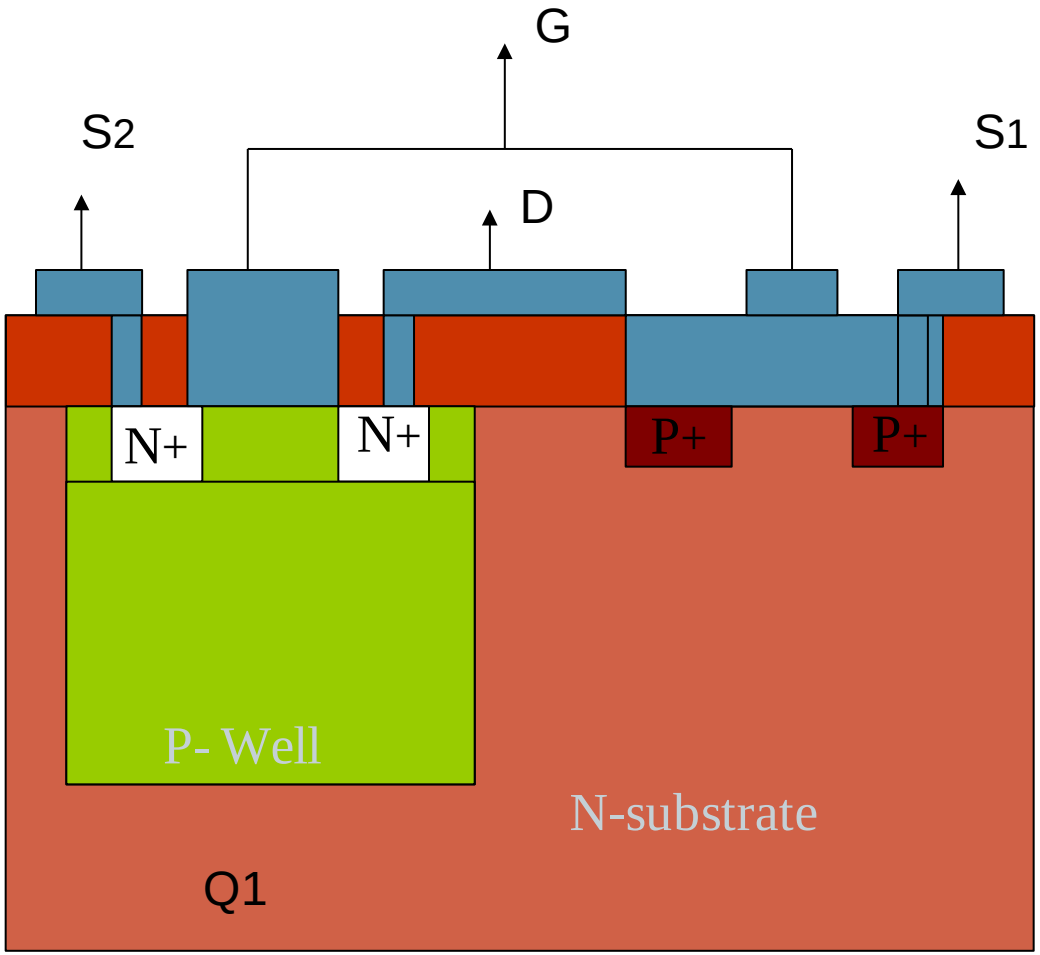
- MOSFET s are very small in size .which make them suitable for highly complex digital arrays

CONSTUCTION OF COMPLEMENTARY MOSFET(CMOS)



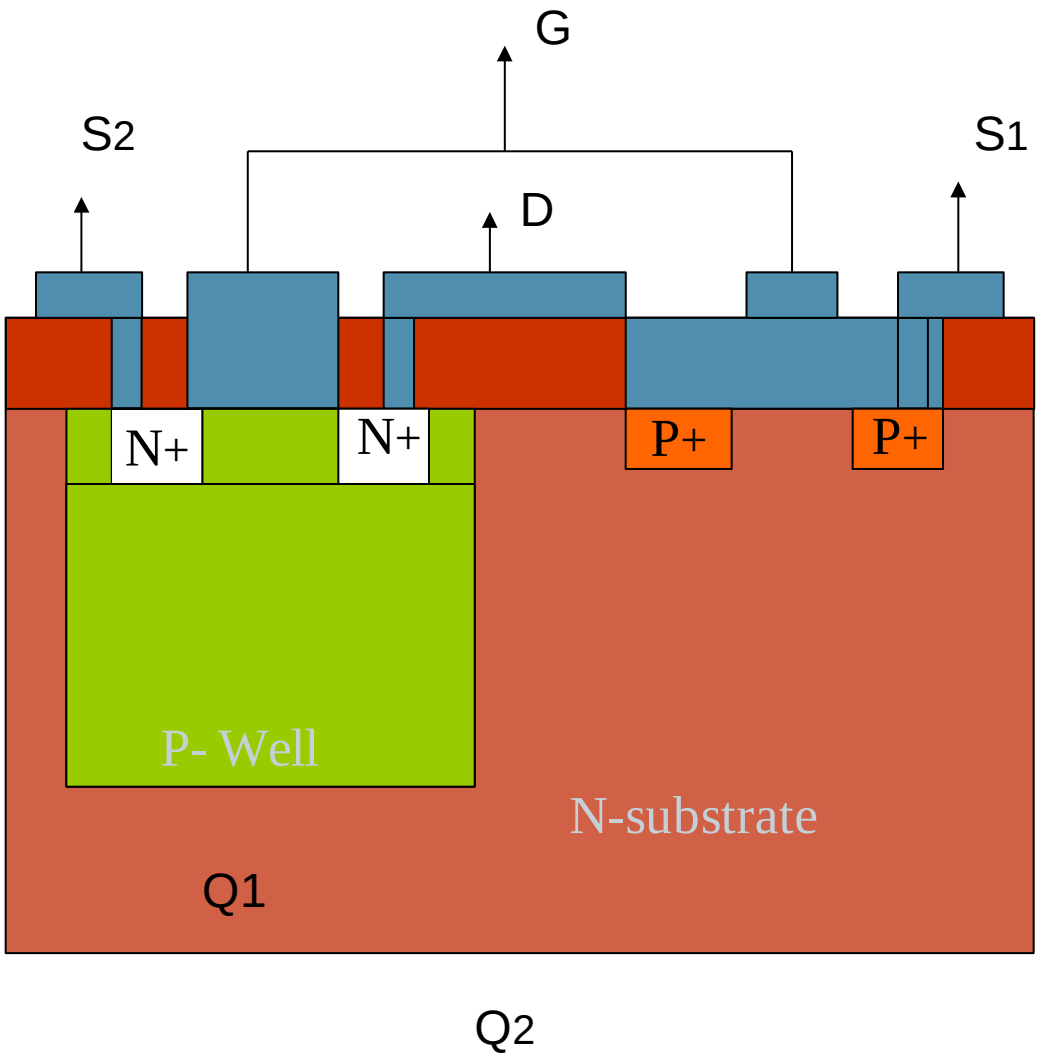
- In this device two MOSFETs that are complementary to each other are used.

CONSTRUCTION OF CMOSFET(contd..)



- The drains of both the MOSFETs are combined and single terminal is taken.

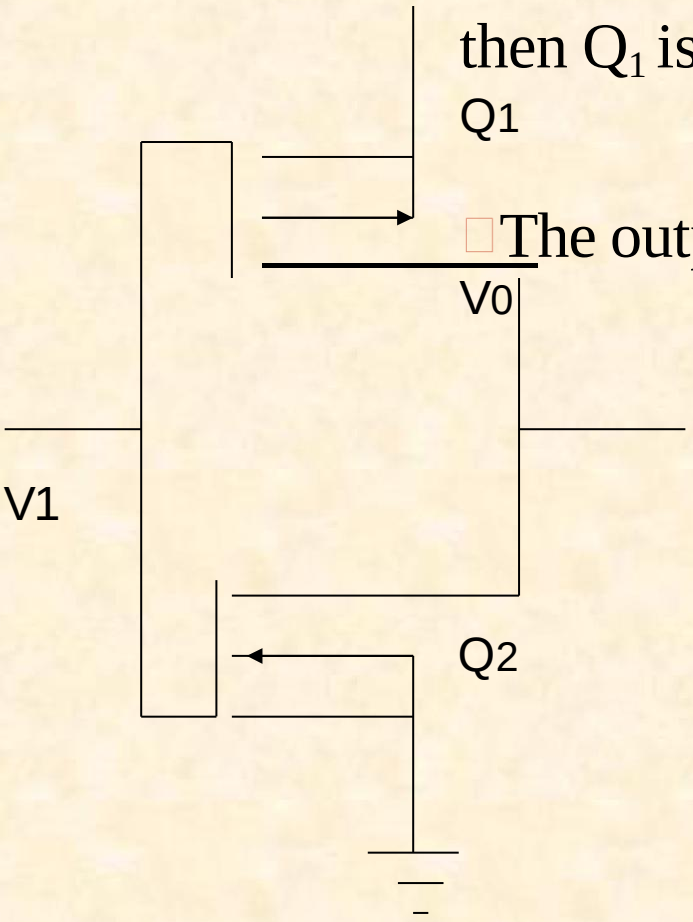
CONSTRUCTION OF CMOSFET(contd..)



- Similarly the gates of both the transistors are combined and a single gate terminal is taken out.

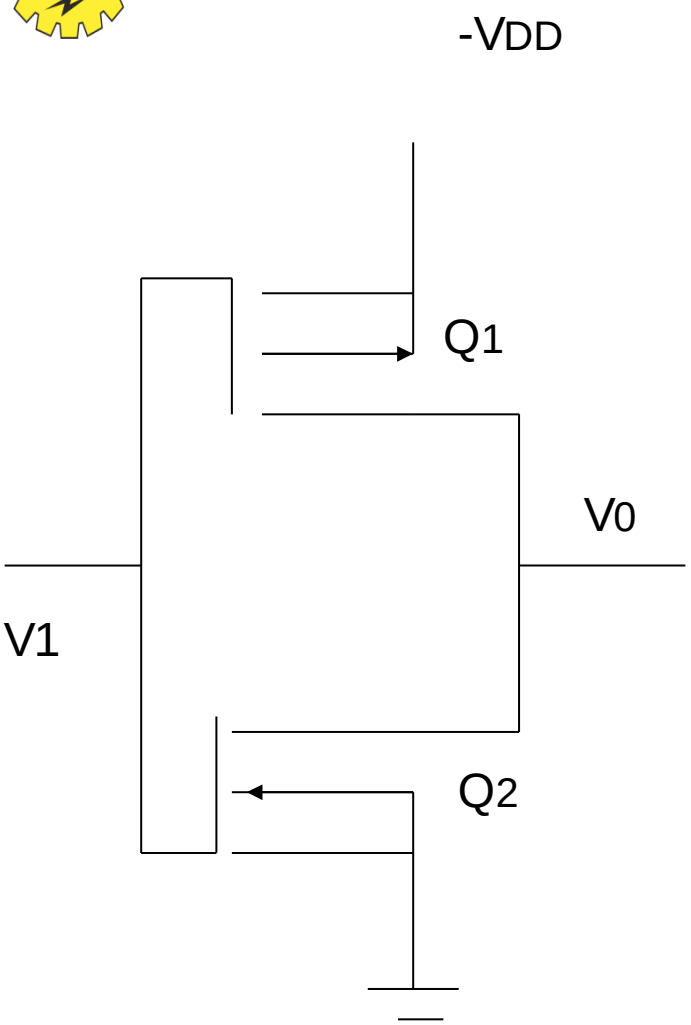
- Here the input is appllied at the input terminal v_i.

WORKING PRINCIPLE OF CMOSFET

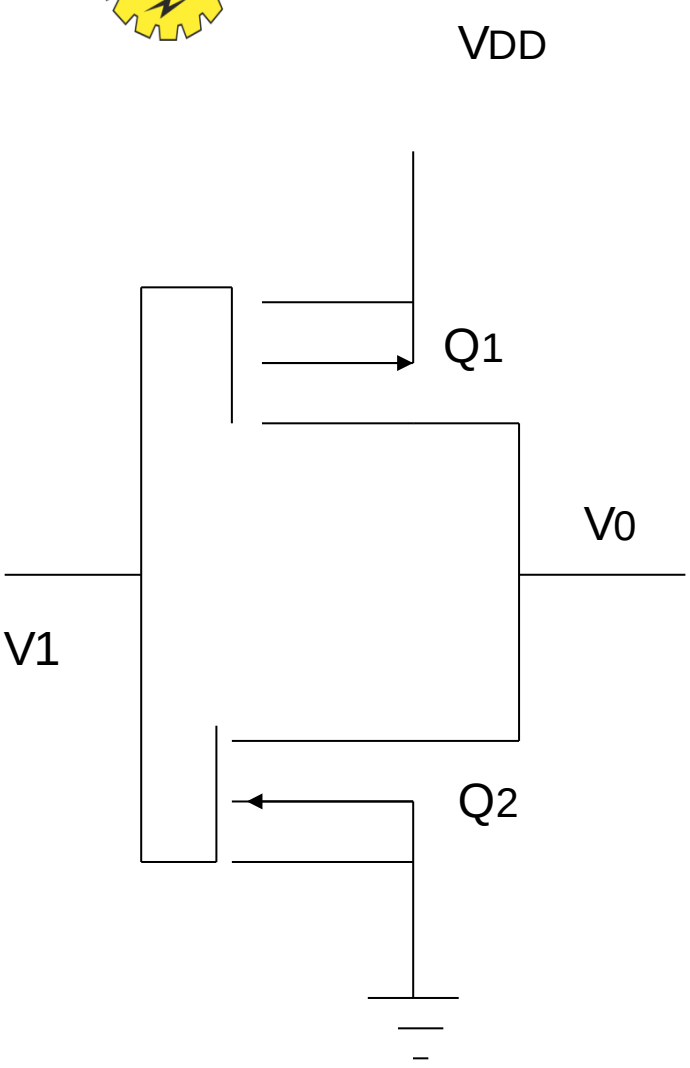


- When v_i is high i.e., equal to $-V_{DD}$ then Q_1 is turned ON and Q_2 is turned OFF.
- The output V_O is zero.
- Similarly when the input voltage Vi is low i.e., equal to 0v, the Q_2 turned ON and Q_1 turned OFF.

WORKING PRINCIPLE OF CMOSFET(contd..)



- So the output voltage Vo lies at –V dd level i.e., high.
- Thus the CMOSFET in this configuration works as an inverter.



•The key advantage of using CMOS design is this extremely low power consumption usually of the order of 50*mv*


THANK YOU