SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

TOPIC 8 –STICK DIAGRAM

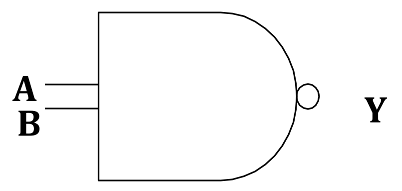
OUTLINE

- INTRODUCTION
- CMOS INVERTER
- MAPPING:STICK DIAGRAM -> CMOS TRANSISTOR CIRCUIT
- NMOS INVERTER-STICK DIAGRAM
- STATIC CMOS NAND GATE
- STATIC CMOS NOR GATE
- STATIC CMOS EXAMPLES-2 STYLES
- ACTIVITY
- EULER PATH
- YOUTUBE VIDEO
- ASSESSMENT

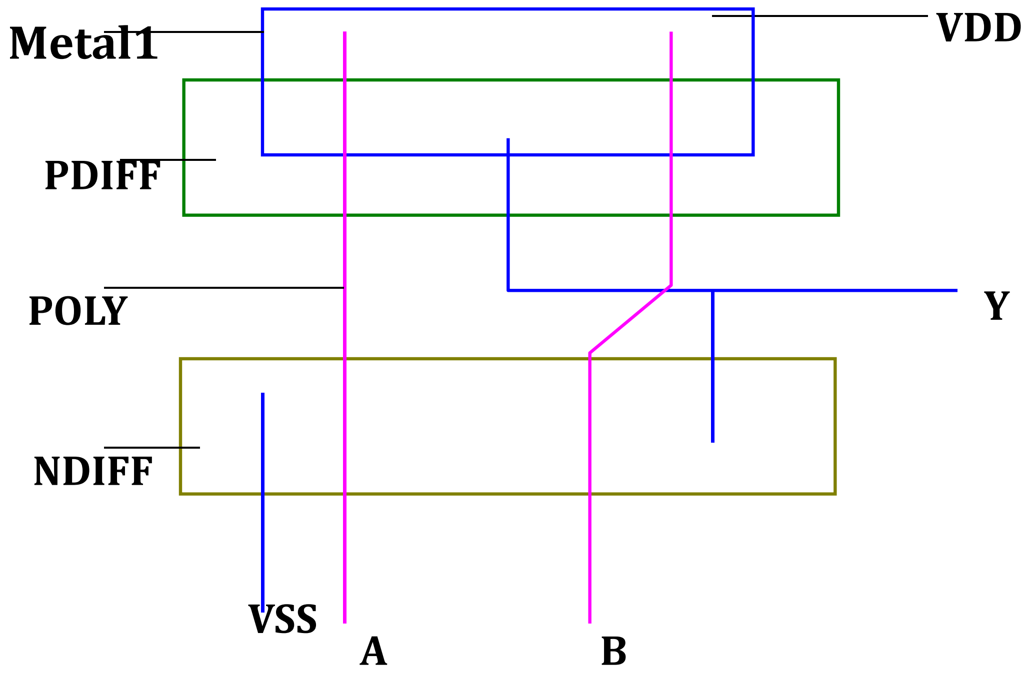
STICK DIAGRAMS-INTRODUCTION

- Intermediate representation between circuit diagram and layout
- Symbolic design is "Sticks" layout.
- Metal-wire
- VDD-power supply
- POLY-Polysilicon (Gate)
- NDIFF-N diffusion(Source)
- PDIFF-P diffusion(Drain)
- VSS-Ground
- A,B-Input
- Y-Output

SYMBOL

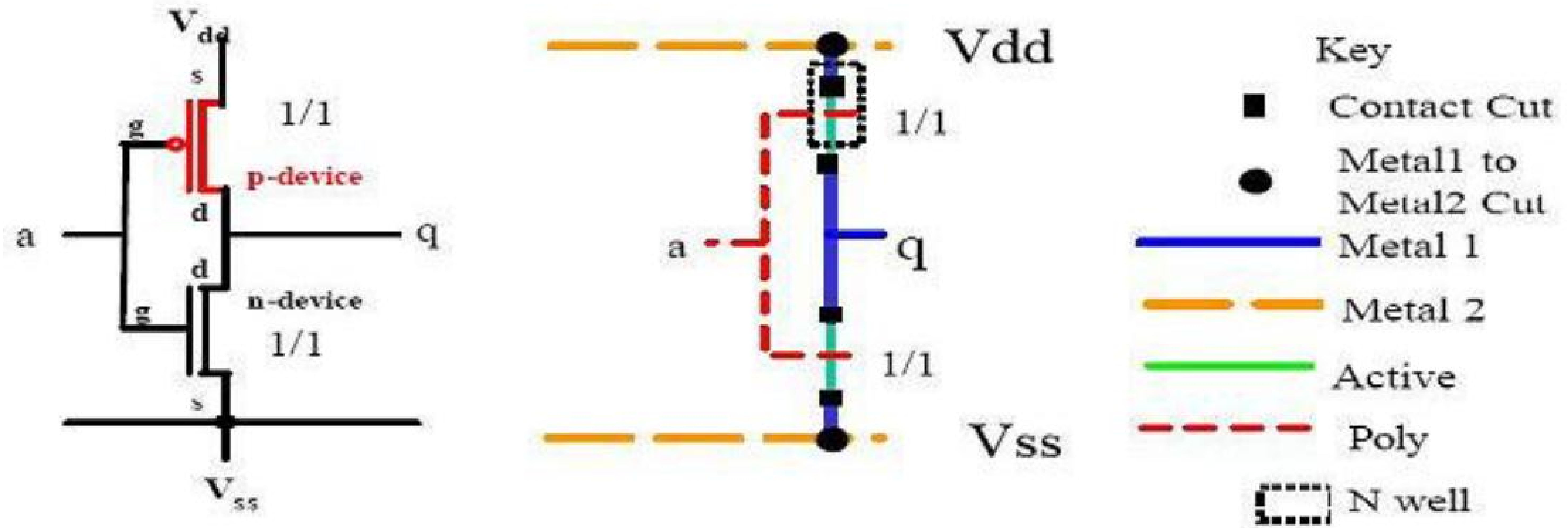


Wp = 5u
Wn = 2.5u

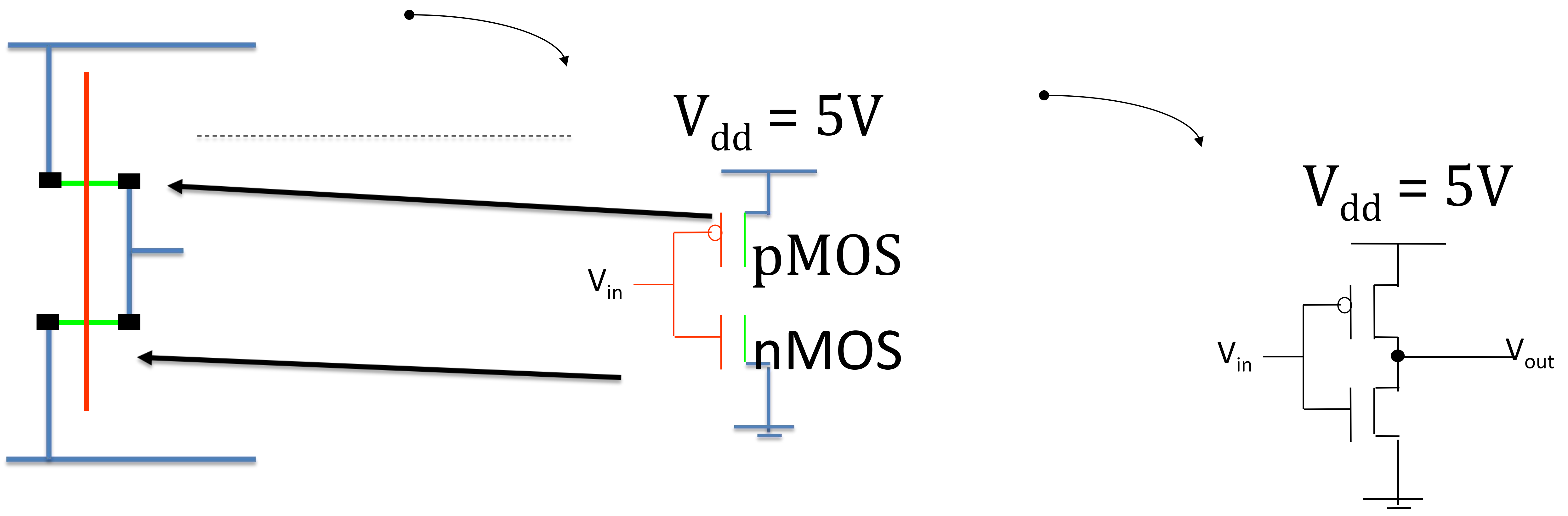


Symbol and Stick Diagram of 2 inputs NAND gate

CMOS INVERTER STICK DIAGRAM

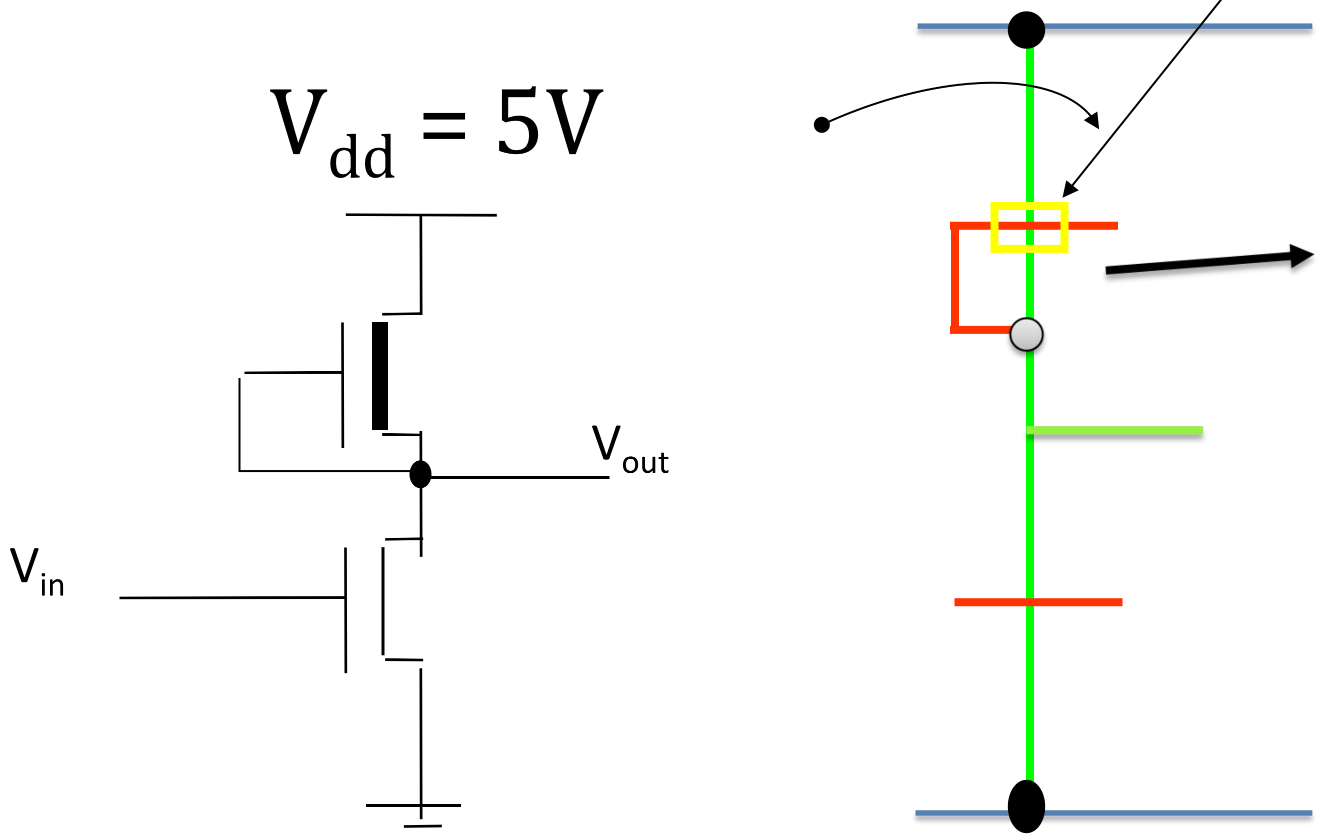


MAPPING:STICK DIAGRAM -> CMOS TRANSISTOR CIRCUIT

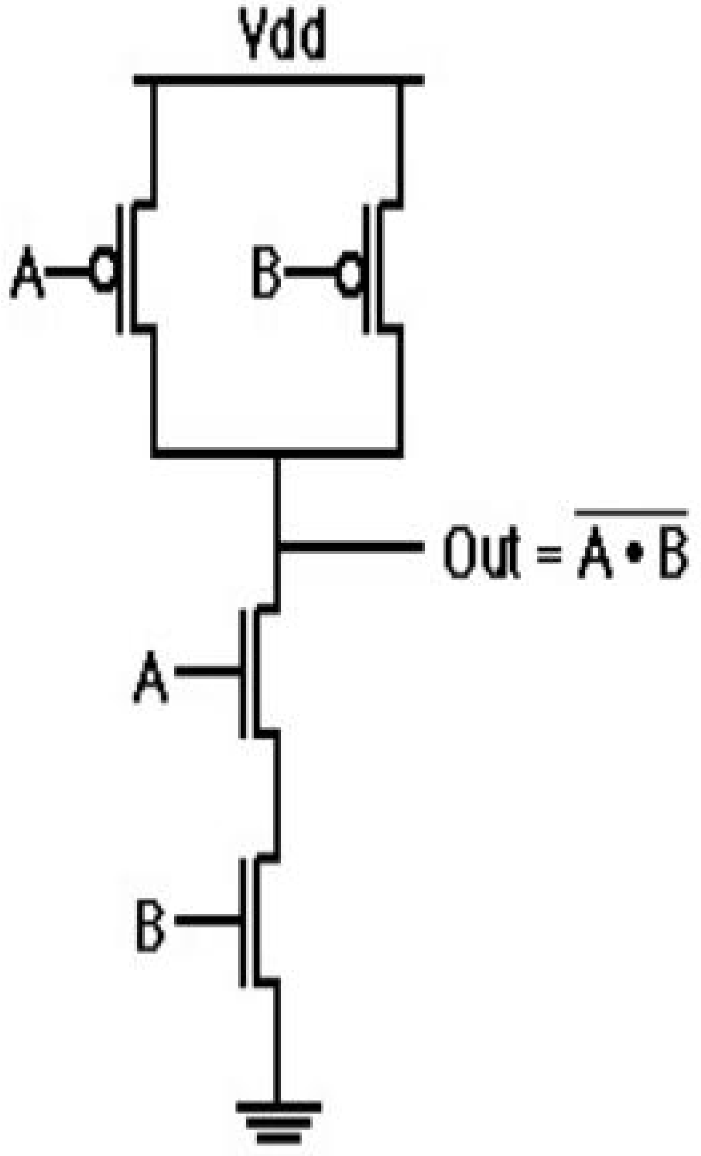


NMOS INVERTER COLOURED STICK DIAGRAM

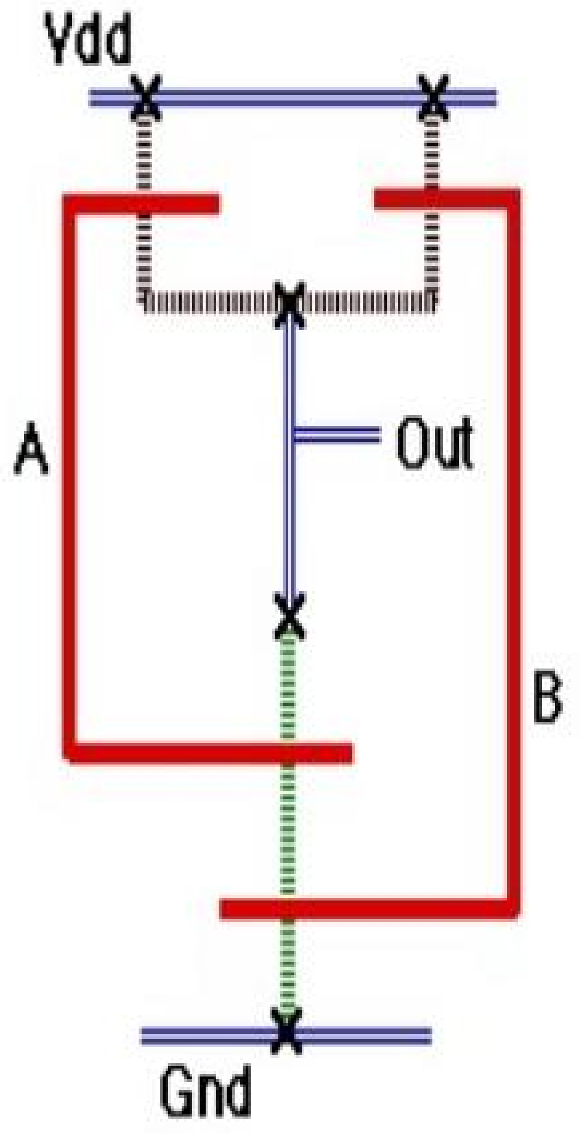
* Note the depletion mode device



STATIC CMOS NAND GATE

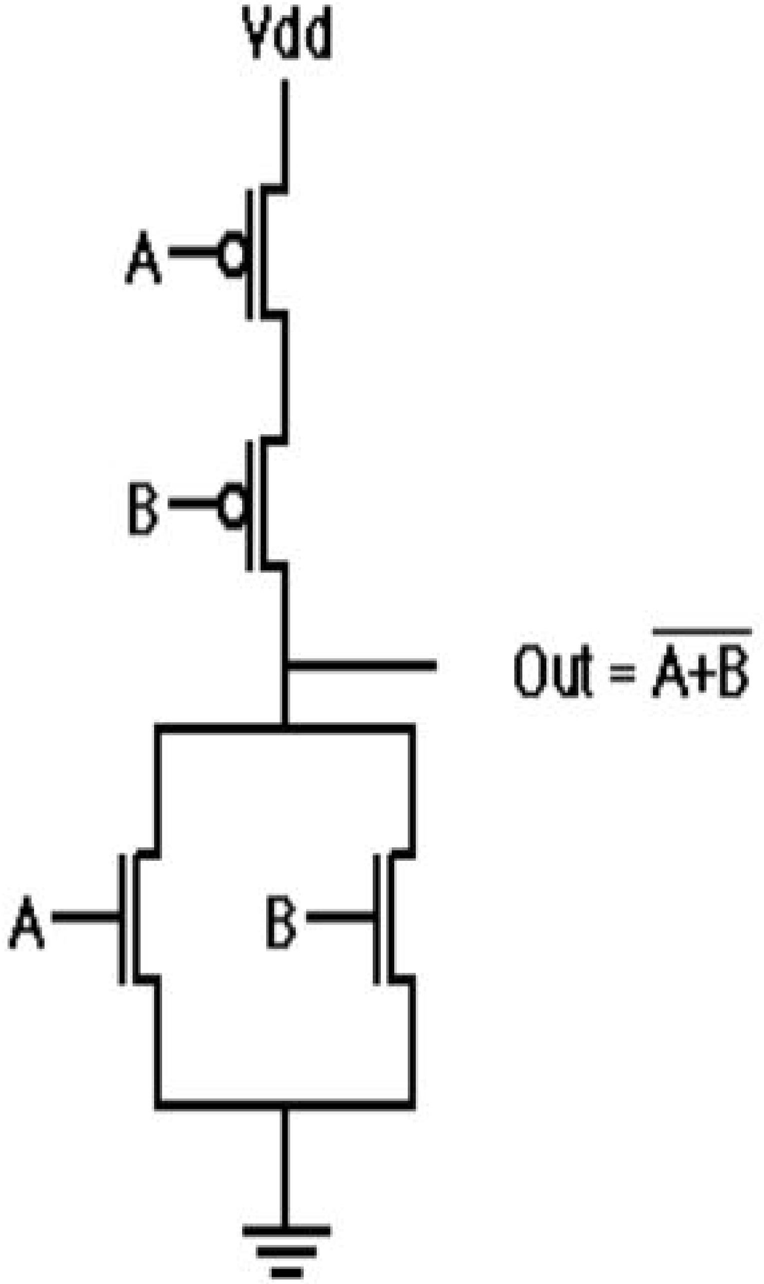


A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

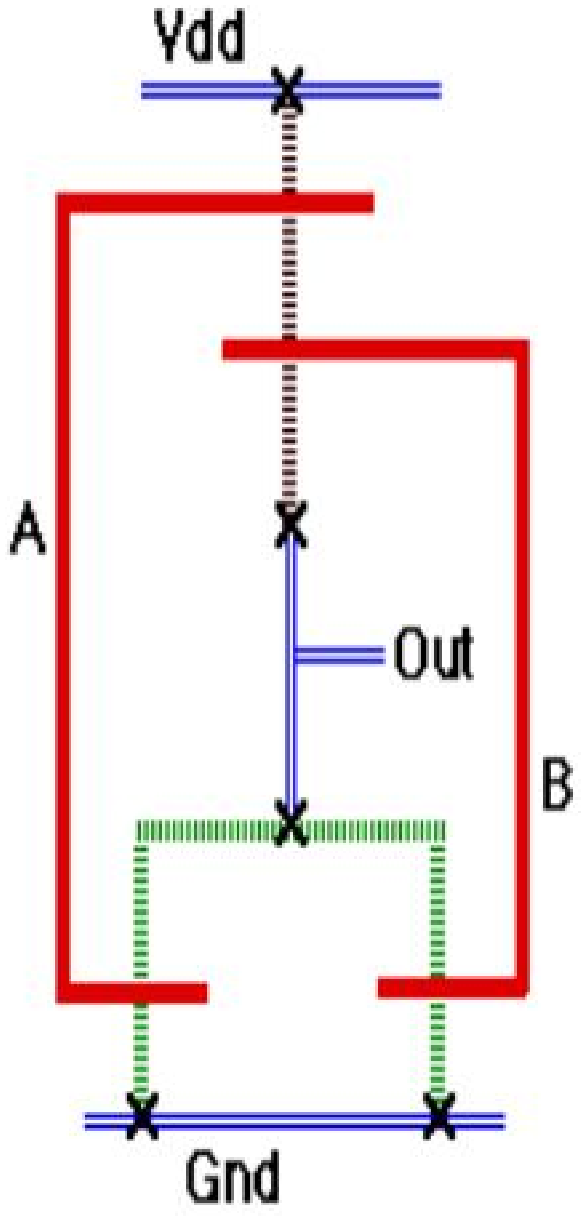


--Pull Down: Connect to ground If A=1 AND B=1
--Pull Up: Connect to VDD If A=0 OR B=0

STATIC CMOS NOR GATE



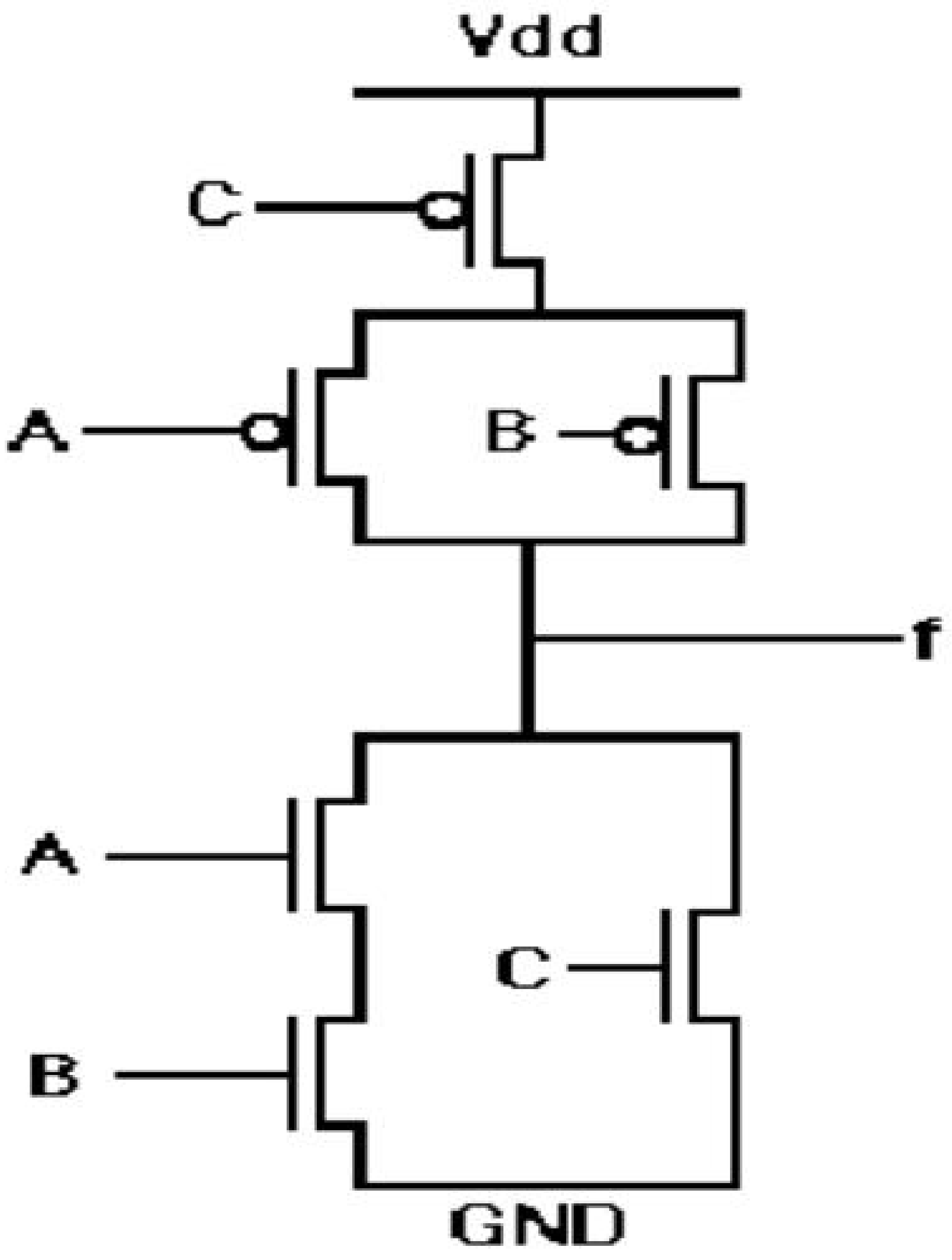
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

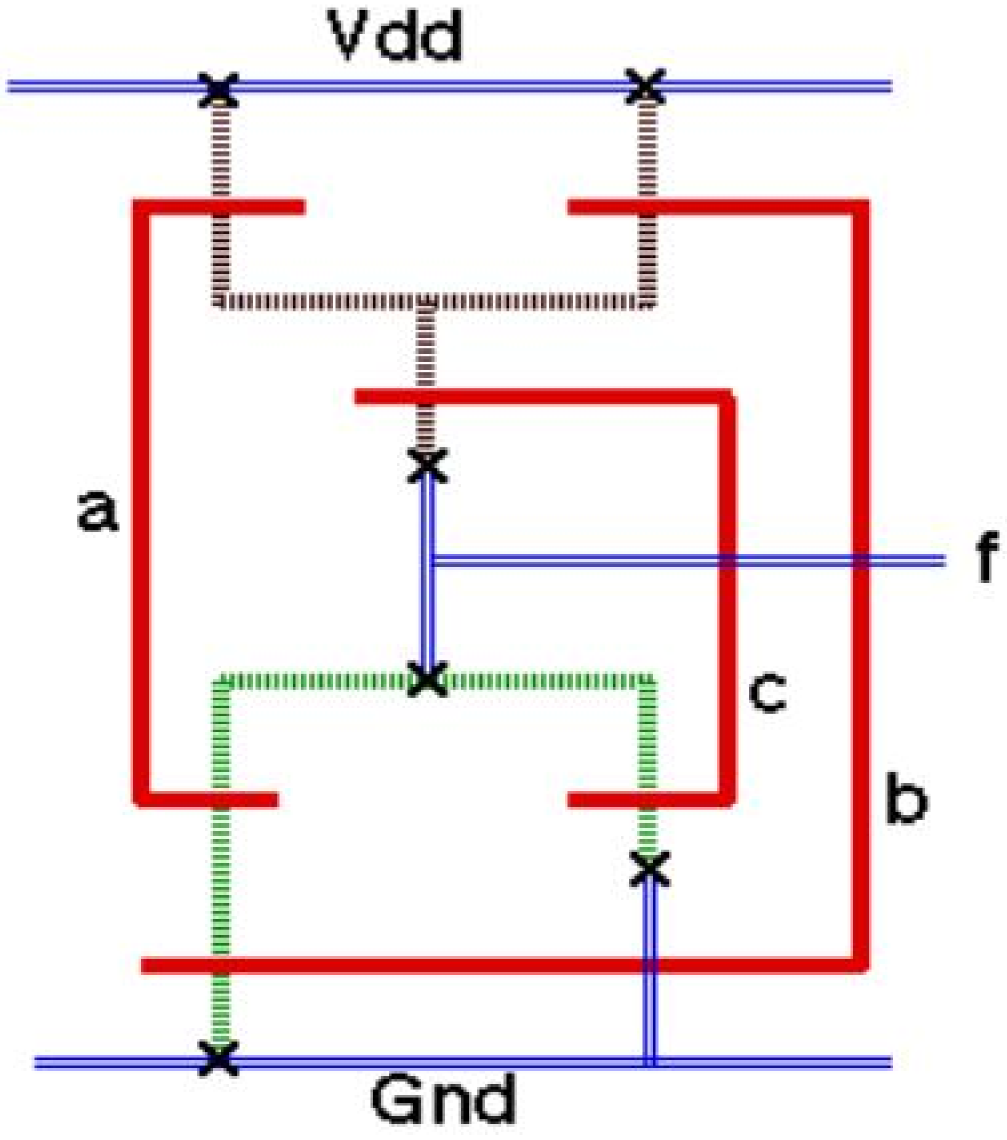


--Pull Down:
Connect to ground If A=1 OR B=1

--Pull Up:
Connect to VDD If A=0 AND B=0

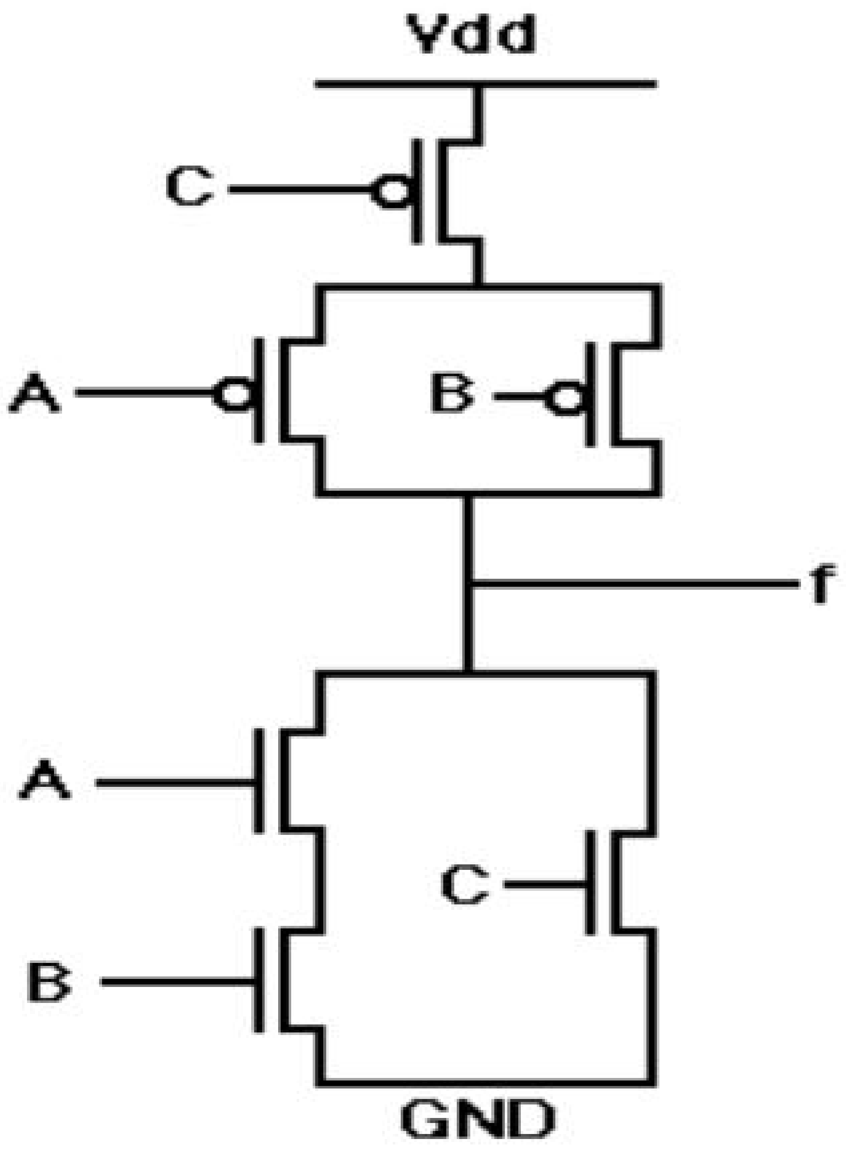
STATIC CMOS DESIGN EXAMPLE STICK DIAGRAM

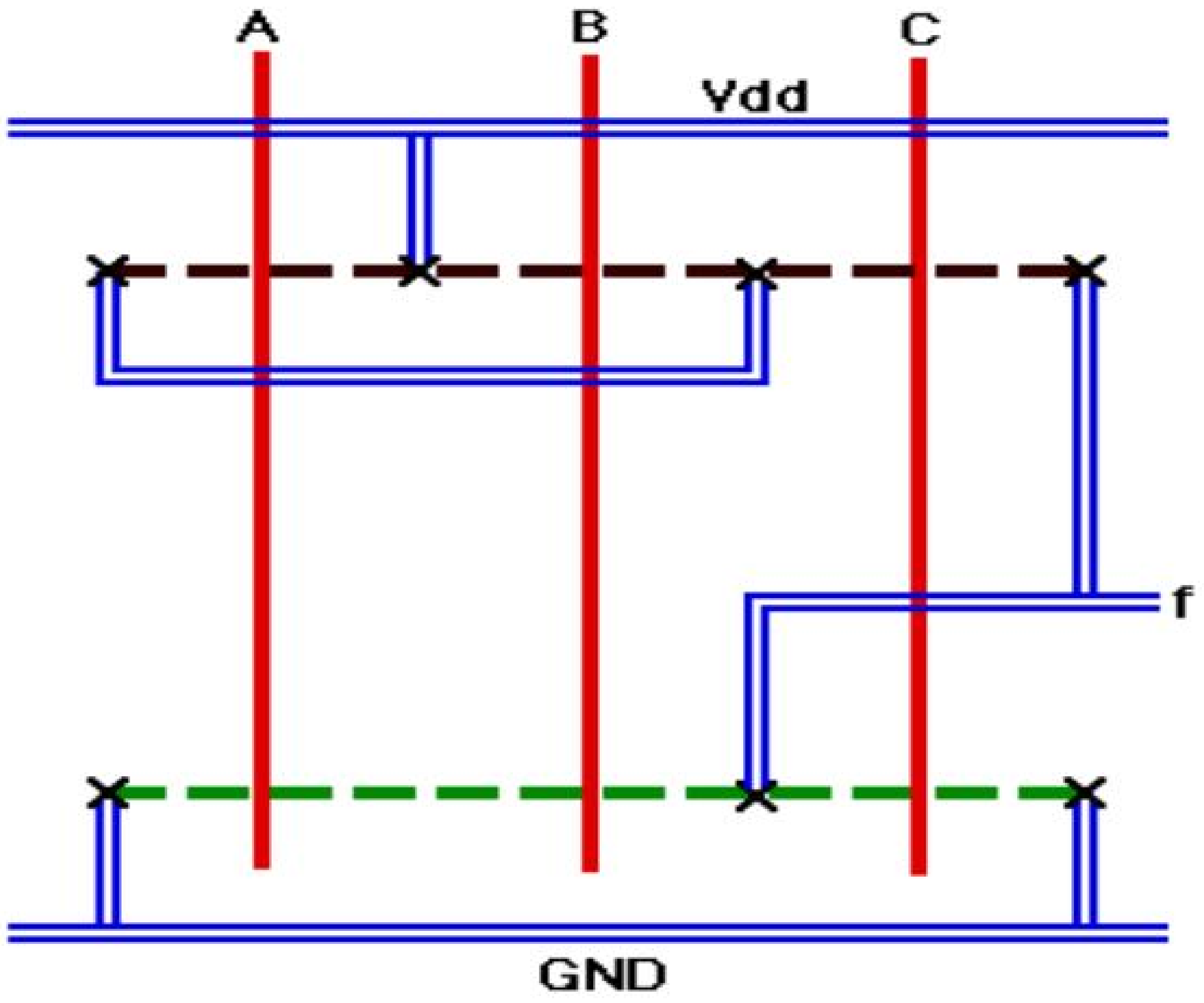




Example: $f = \overline{a \bullet b + c}$

STICK DIAGRAM 2 (DIFFERENT LAYOUT STYLE TO PREVIOUS BUT SAME FUNCTION BEING IMPLEMENTED





Example: $f = \overline{(A \cdot B) + C}$

COMPLEX LOGIC GATES LAYOUT

EX: F=AB+E+CD

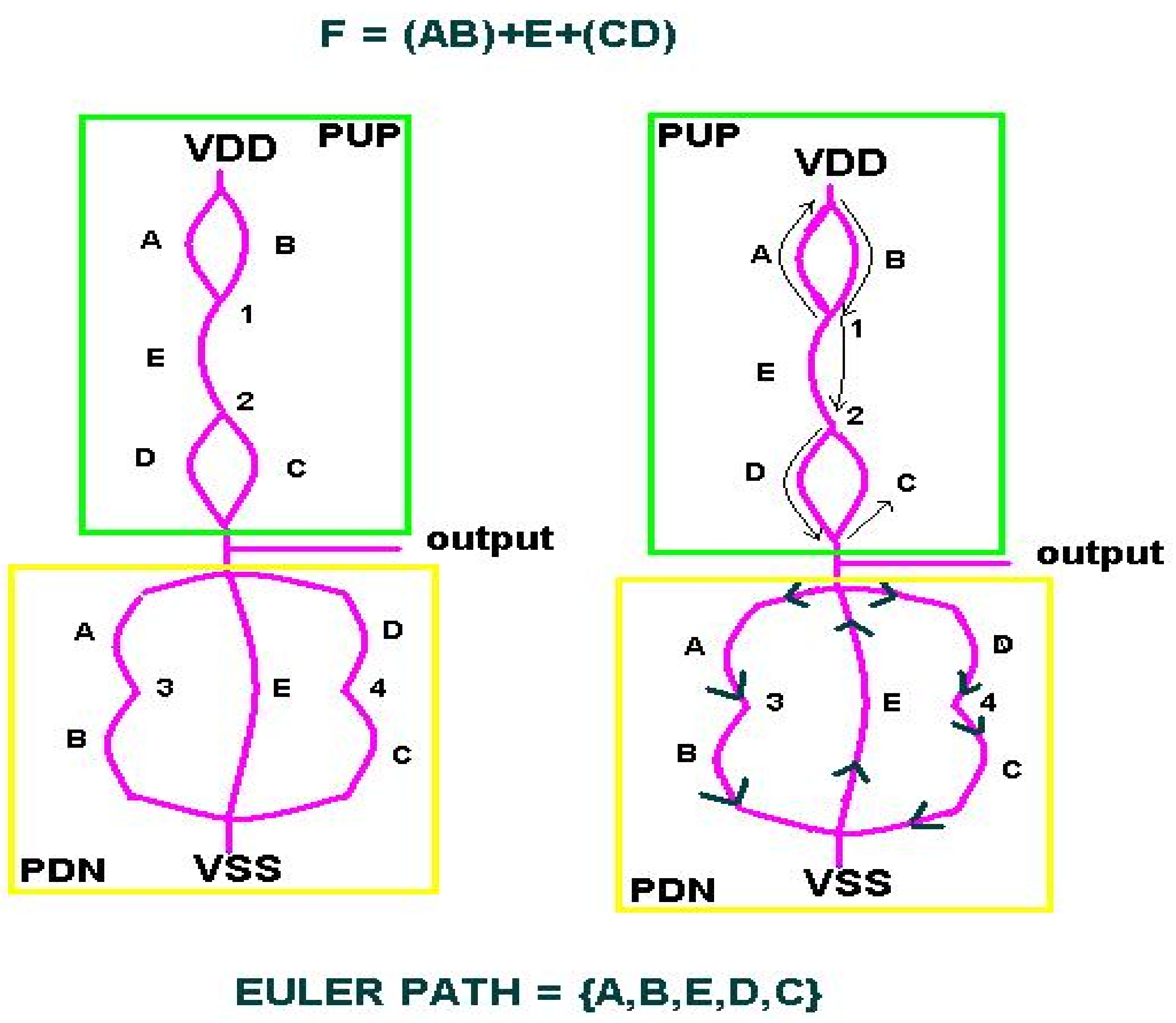
Euler paths

Circuit to graph (convert)

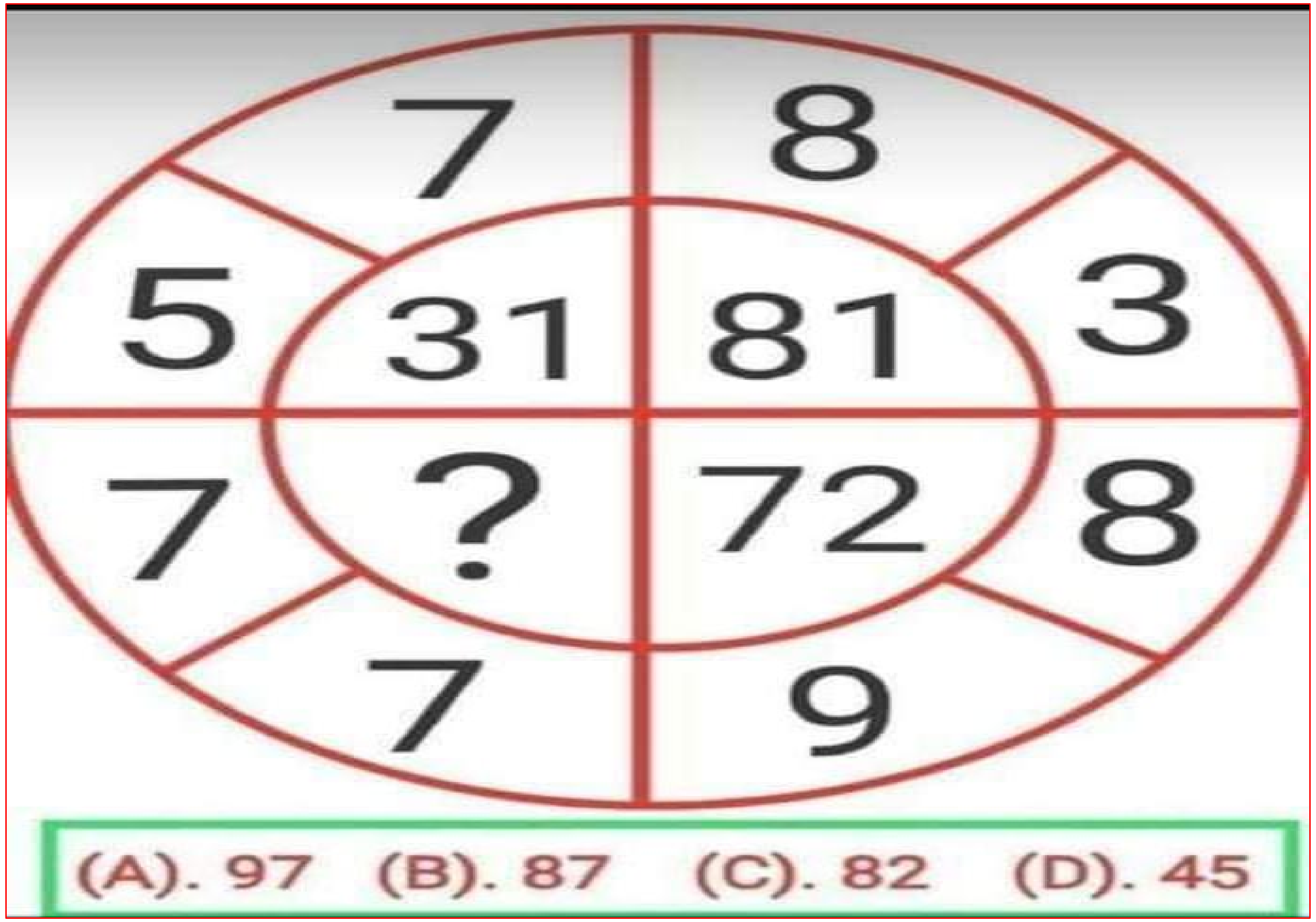
1) Vertices are source/Drain connections

2) Edges are transistors

Find p and n Euler paths

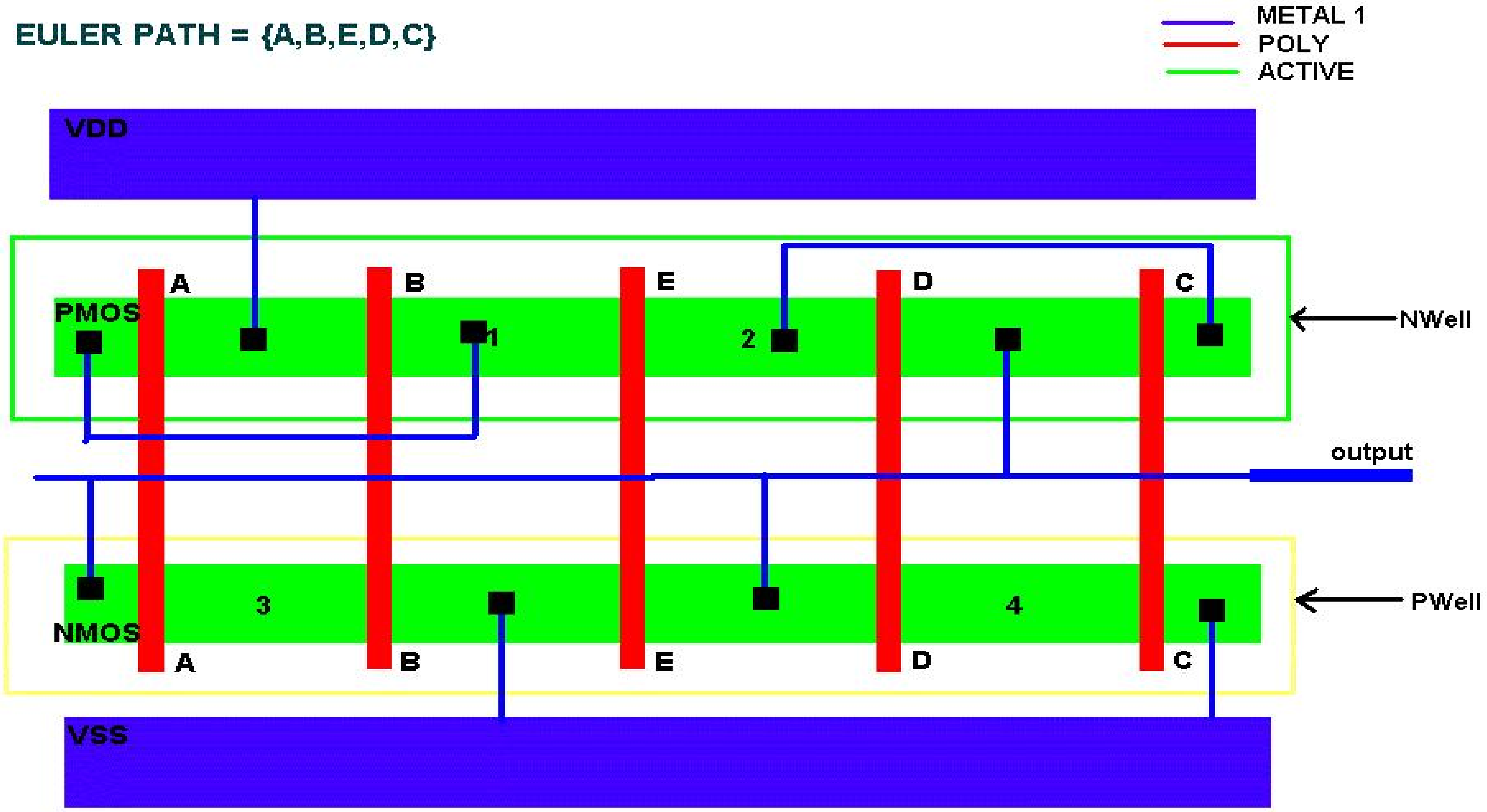


CLASS ROOM ACTIVITY



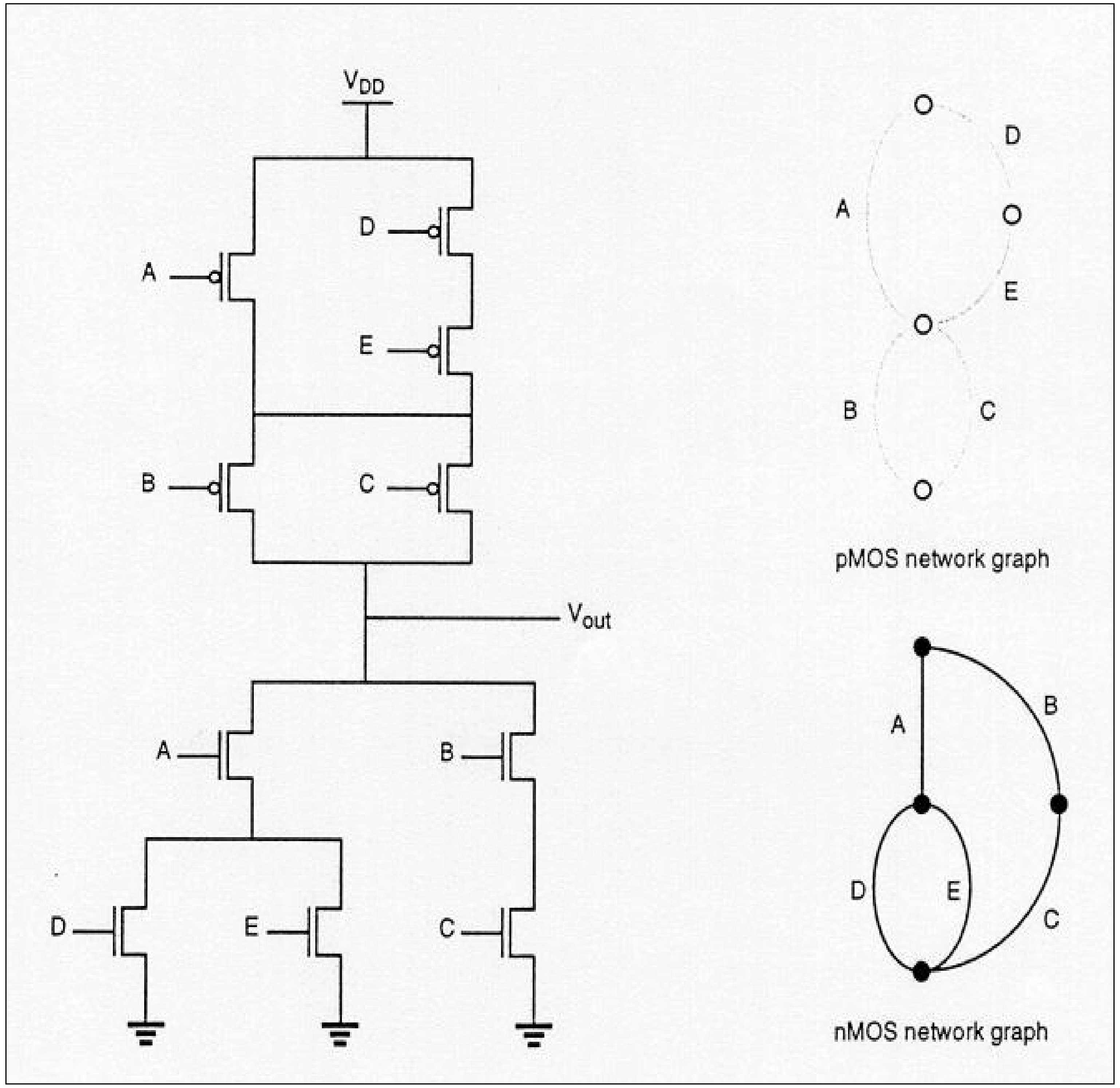
EULER PATH

EULER PATH = {A,B,E,D,C}

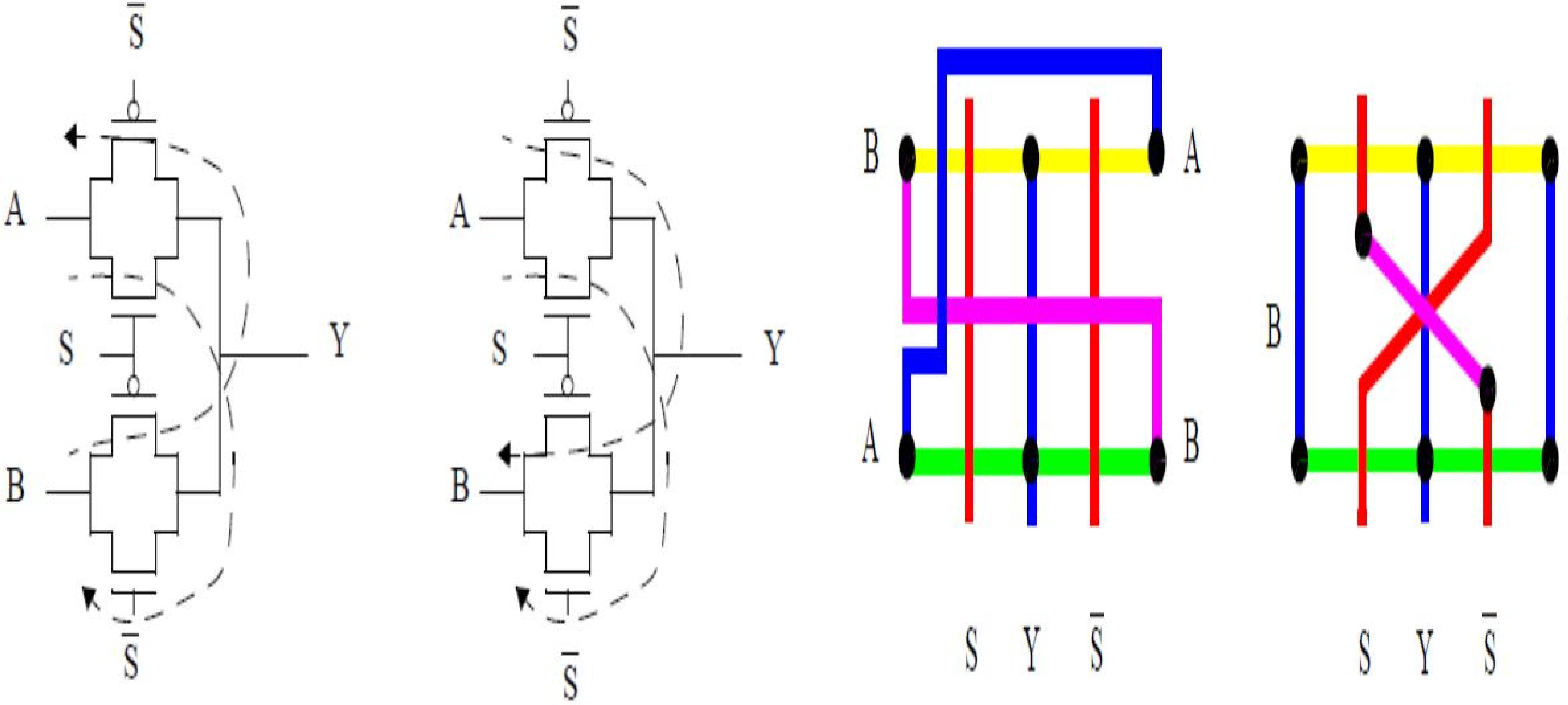


PMOS & NMOS

- This notation indicates only the relative positioning of the various design components.
- The absolute coordinates of these elements are determined automatically by the editor using a compactor.
- The compactor translates the design rules into a set of constraints on the component positions, and solve a constrained optimization problem that attempts to minimize the area or cost function.



EULER GRAPH-STICK DIAGRAM COMPARISON

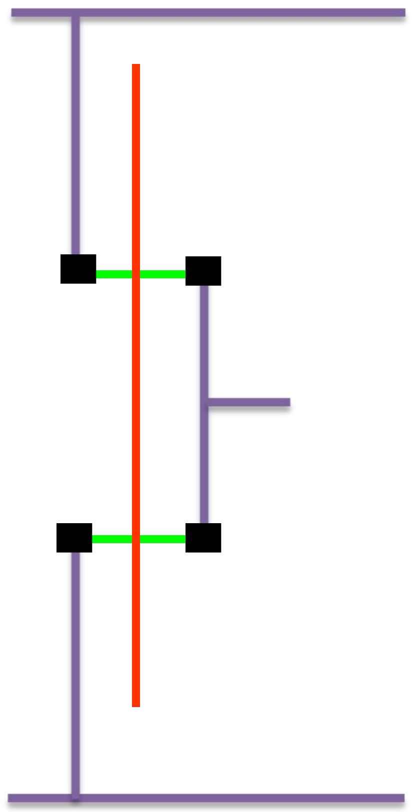


YOUTUBE VIDEO LINK

STICK DIAGRAM - simplified (VLSI)
https://www.youtube.com/watch?v=wqRGa5sOUmc&t=212s

ASSESSMENT-
CMOS INVERTER COLOURED STICK DIAGRAM

1.DRAW THE CMOS INVERTER STICK DIAGRAM
2.DRAW THE CMOS NAND GATE



3.TELL ME THE COLOR CODING NAME ????????

ADVANTAGE & DISADVANTAGE

- **ADVANTAGE :** Designer does not have to worry about design rules, because the compactor ensures that the final layout is physically correct.
- **DISADVANTAGE :** The outcome of the compaction phase is often unpredictable. The resulting layout can be less dense than what is obtained with the manual approach.It does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

To easy remember .n s
Dot-NAND, n-NMOS,S-Series

SUMMARY & THANK YOU