SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

11/24/2023

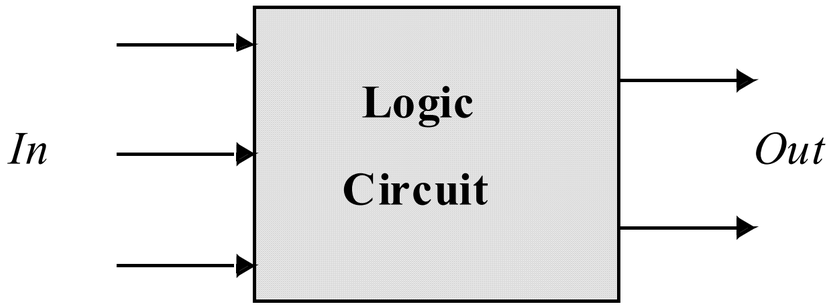
UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC 1–EXAMPLES OF COMBINATIONAL LOGIC DESIGN

OUTLINE

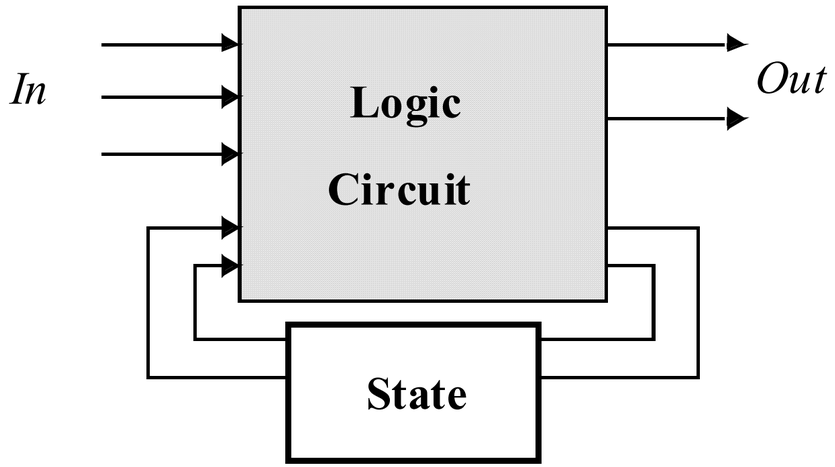
- COMBINATIONAL VS. SEQUENTIAL LOGIC
- CMOS CIRCUIT
- NMOS & PMOS IN SERIES & PARALLEL
- DEMORGANS THEOREM
- EXAMPLES:NOR & NAND
- ACTIVITY
- COMPLEX LOGIC GATE
- NMOS OPERATION
- EXAMPLES OF COMBINATIONAL LOGIC
- FULL ADDER,CARRY SKIP ADDER
- DECODER
- ASSESSMENT
- SUMMARY & THANK YOU

COMBINATIONAL VS. SEQUENTIAL LOGIC



(a) Combinational

Output = *f*(*In*)

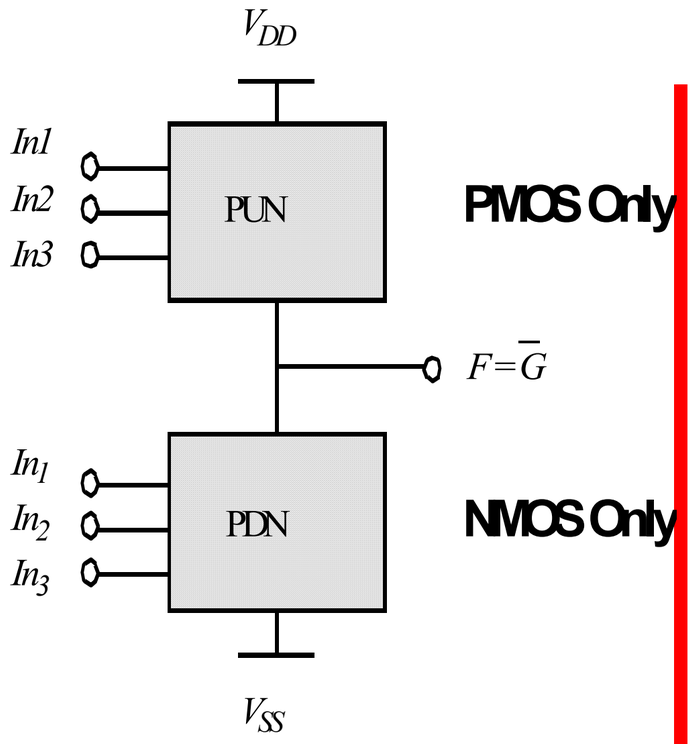


(b) Sequential

Output = *f*(*In, Previous In*)

CMOS CIRCUIT

- At every point in time (except during the switching transients) each gate output is connected to either V_{DD} or V_{ss} via a low-resistive path.
- The outputs of the gates assume at all times the value of the Boolean function, implemented by the circuit (ignoring, once again, the transient effects during switching periods).
- This is in contrast to the dynamic circuit class ,which relies on temporary storage of signal values on the capacitance of high impedance circuit nodes.



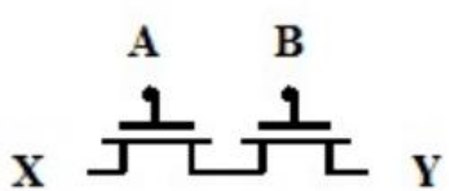
PUN and PDN are Dual Networks

NMOS TRANSISTORS IN SERIES/PARALLEL CONNECTION

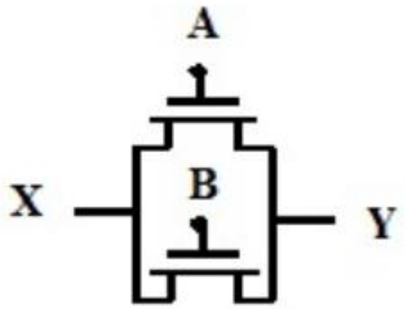
•Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is **HIGH**

•NMOS passes strong 0 but a weak 1



Y=X ; If A AND B

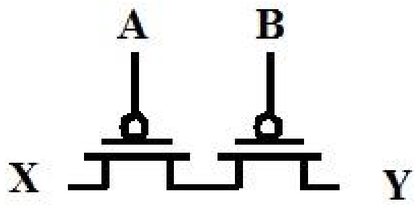


Y=X ; If A OR B

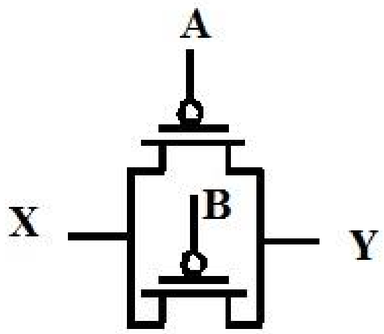
PMOS TRANSISTORS IN SERIES/PARALLEL CONNECTION

PMOS switch closes when switch control input is **LOW**

- NMOS passes strong 1 but a weak 0



Y=X ; If A bar AND B bar



Y=X ; If A bar OR B bar

COMPLEMENTARY CMOS LOGIC STYLE CONSTRUCTION

- DEMORGANS THEOREM

$$\overline{A+B} = \bar{A}\bar{B}$$

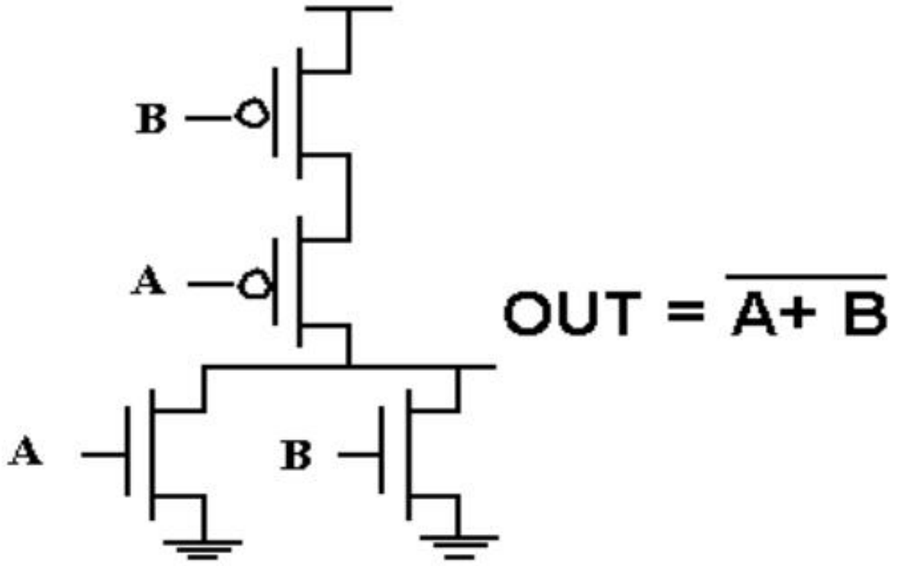
$$\overline{AB} = \bar{A}+\bar{B}$$

- PUP is the DUAL OF PDN
- AND = NAND + INV

EXAMPLE GATE: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

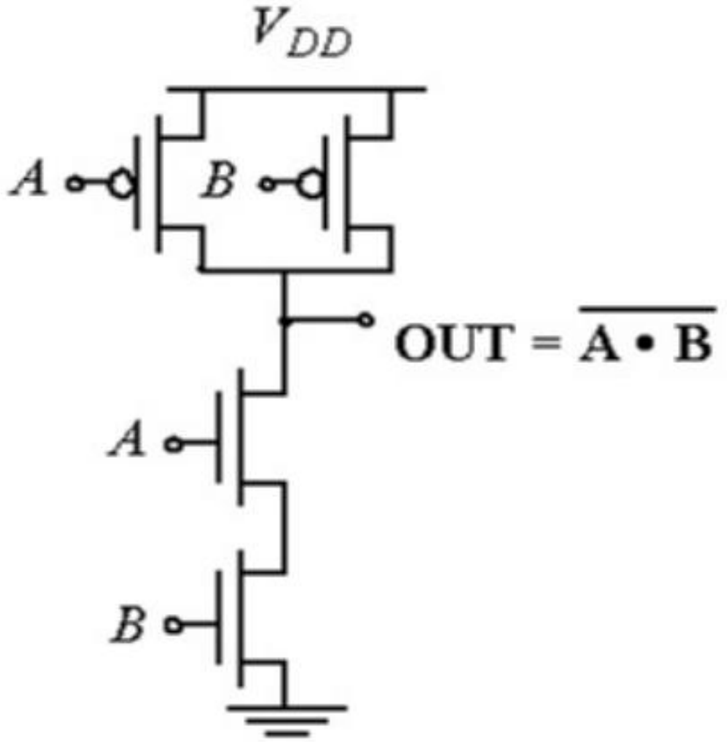
Truth Table of a 2 input NOR gate



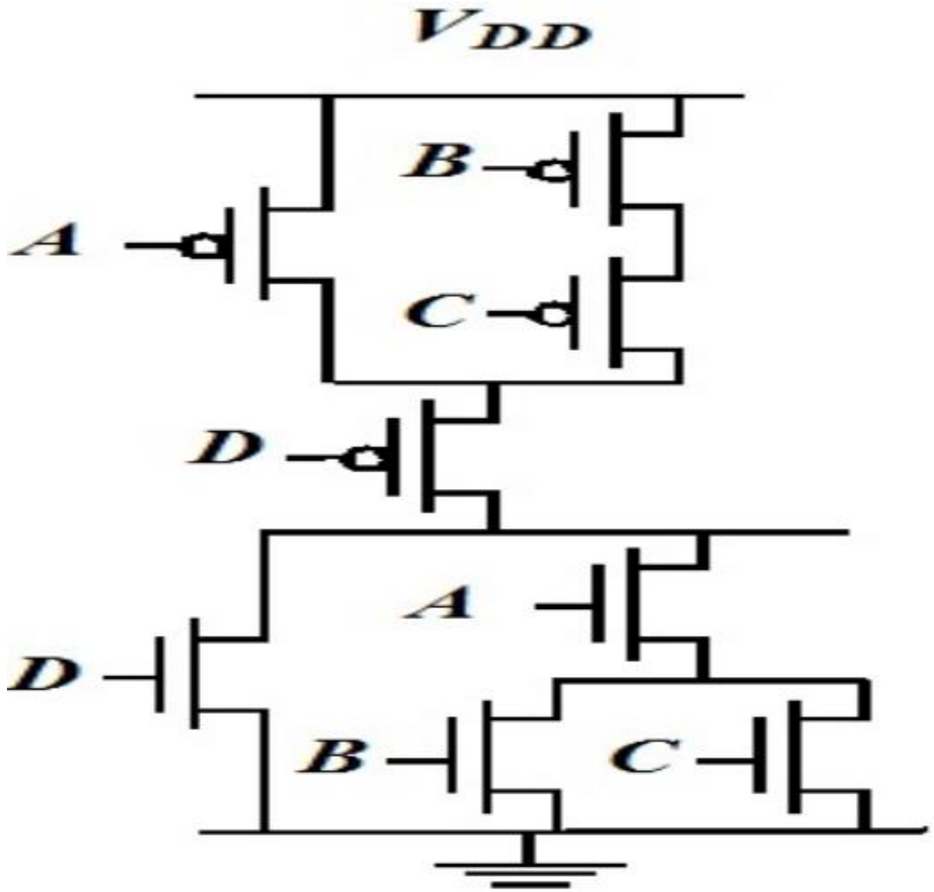
EXAMPLE GATE: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



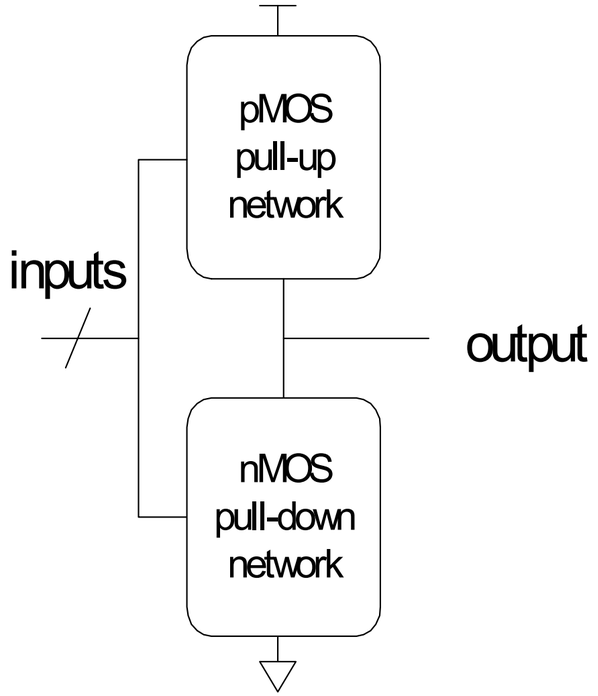
COMPLEX GATE : FIND THE OUTPUT



COMPLEMENTARY CMOS LOGIC GATES

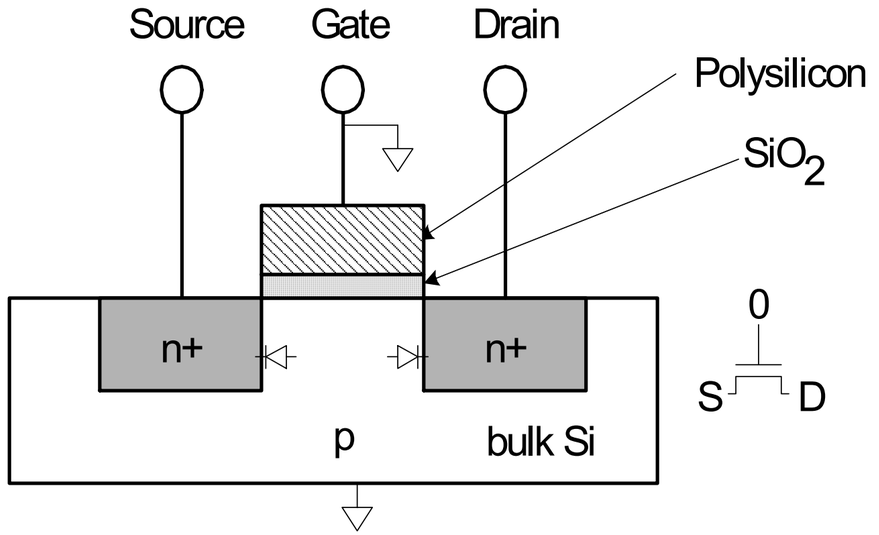
- nMOS pull-down network
- pMOS pull-up network
- Eg. static CMOS

	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)



NMOS OPERATION

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



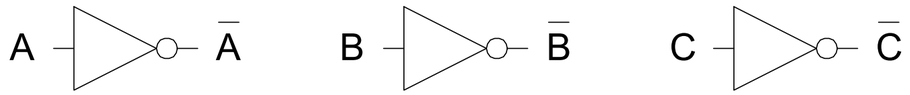
EXAMPLES OF COMBINATIONAL LOGIC

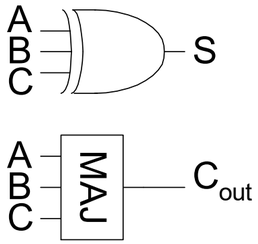
- ADDER

  -HALF ADDER ,FULL ADDER,CARRY SKIP/SAVE/LOOKAHEAD ADDER,

- SUBTRACTOR
- MULTIPLIER
- MUX & DEMUX
- ENCODER & DECODER
- FREQUENCY DIVIDER

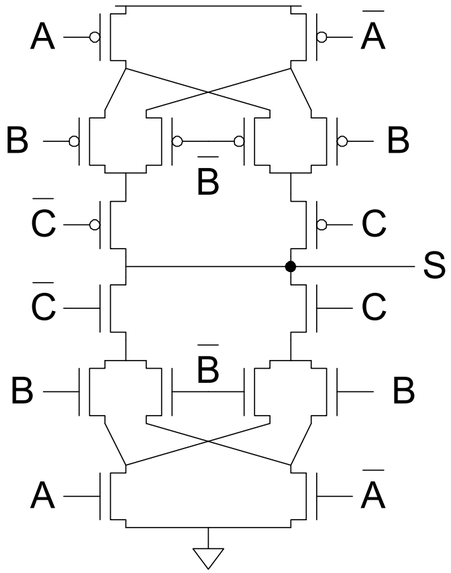
FULL ADDER DESIGN

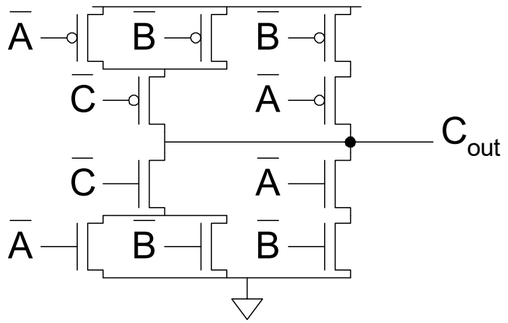




$$S = A \oplus B \oplus C$$

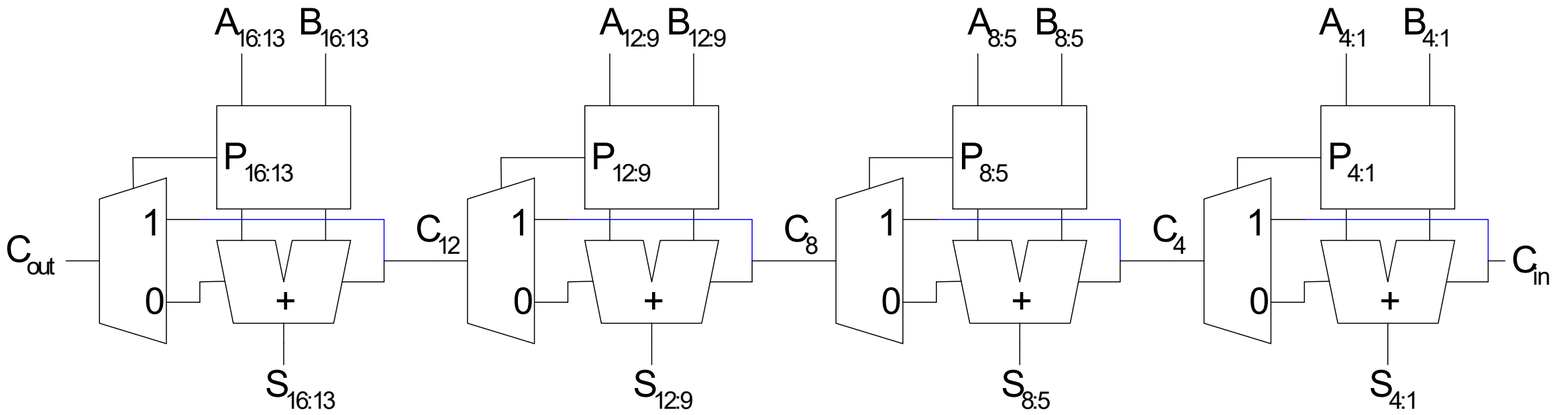
$$C_{out} = MAJ(A,B,C)$$





CARRY-SKIP ADDER

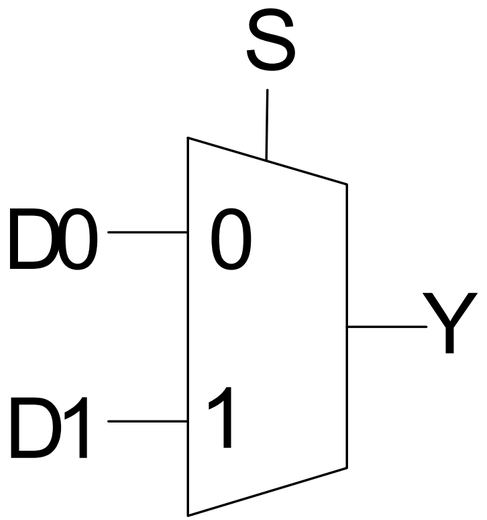
- Carry-ripple is slow through all N stages
- Carry-skip allows carry to skip over groups of n bits
  - -Decision based on n-bit propagate signal



MUX

- 2:1 multiplexer chooses between two inputs

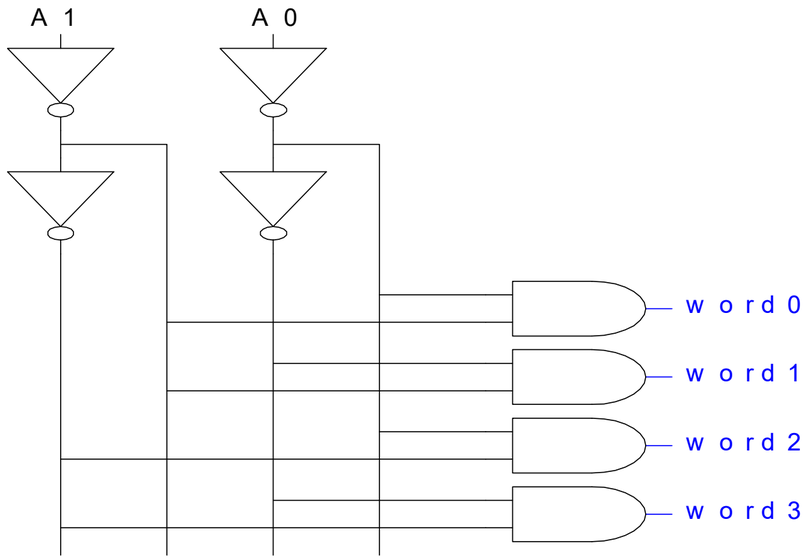
S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

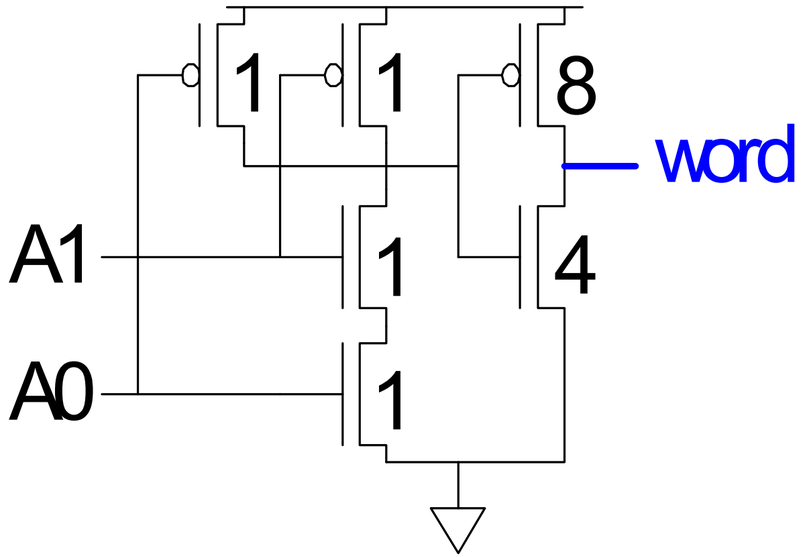


DECODERS

- n:2^n decoder consists of 2^n n-input AND gates
  - One needed for each row of memory
  - Build AND from NAND or NOR gates

Static CMOS





ASSESSMENT

- Design Full Adder using 2 half adder
- Write the derivation of output of 2:1 MUX
- Compare Encoder & decoder
- Differentiate Combinational logic and Sequential logic circuits
- Compare nMOS & pMOS?

SUMMARY & THANK YOU