



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with ‘A+’ Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE CODE & NAME: 19ECB302 VLSI DESIGN

III YEAR/V SEMESTER

UNIT 1- MOS TRANSISTOR PRINCIPLE

**TOPIC 2- BASIC MOS TRANSISTOR ACTION &
CMOS FABRICATION P-WELL PROCESS**



OUTLINE

- Introduction & levels of integration- Moore's law
- Design Abstraction Levels
- Why the name MOS?
- Two mode transistor action
- Activity
- Enhancement mode, Depletion mode
- P-well process with different masking levels
- CMOS P-well Inverter
- Summary

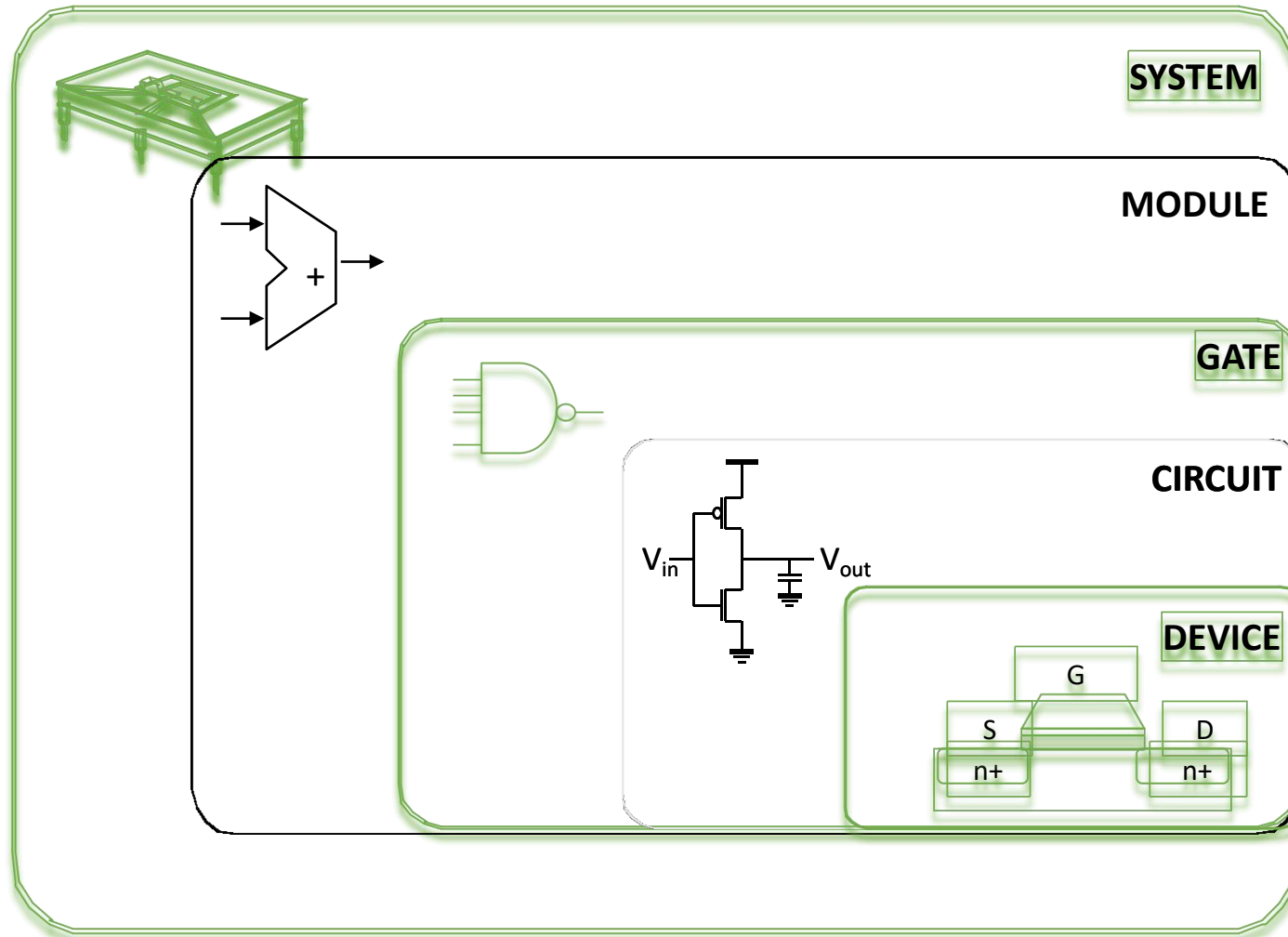


LEVELS OF INTEGRATION

Integration	Transistors	Examples
SSI	10-100	Logic gates
MSI	100-1000	counters
LSI	1000-20000	8-bit chip
VLSI	20000-1000000	16 & 32 bit up
ULSI	1000000- 10000000	Special processors, virtual reality machines, smart sensors



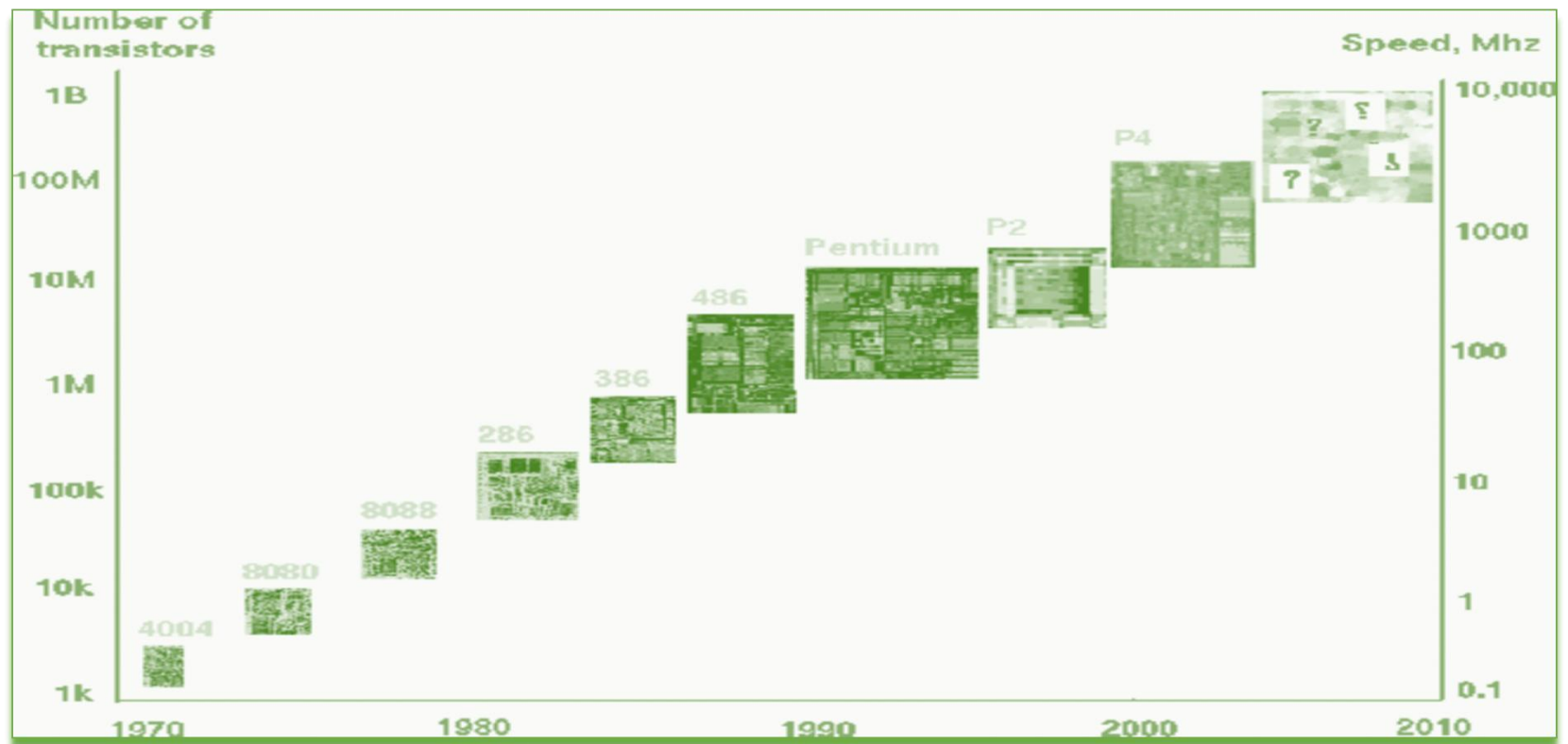
DESIGN ABSTRACTION LEVELS





MOORE'S LAW

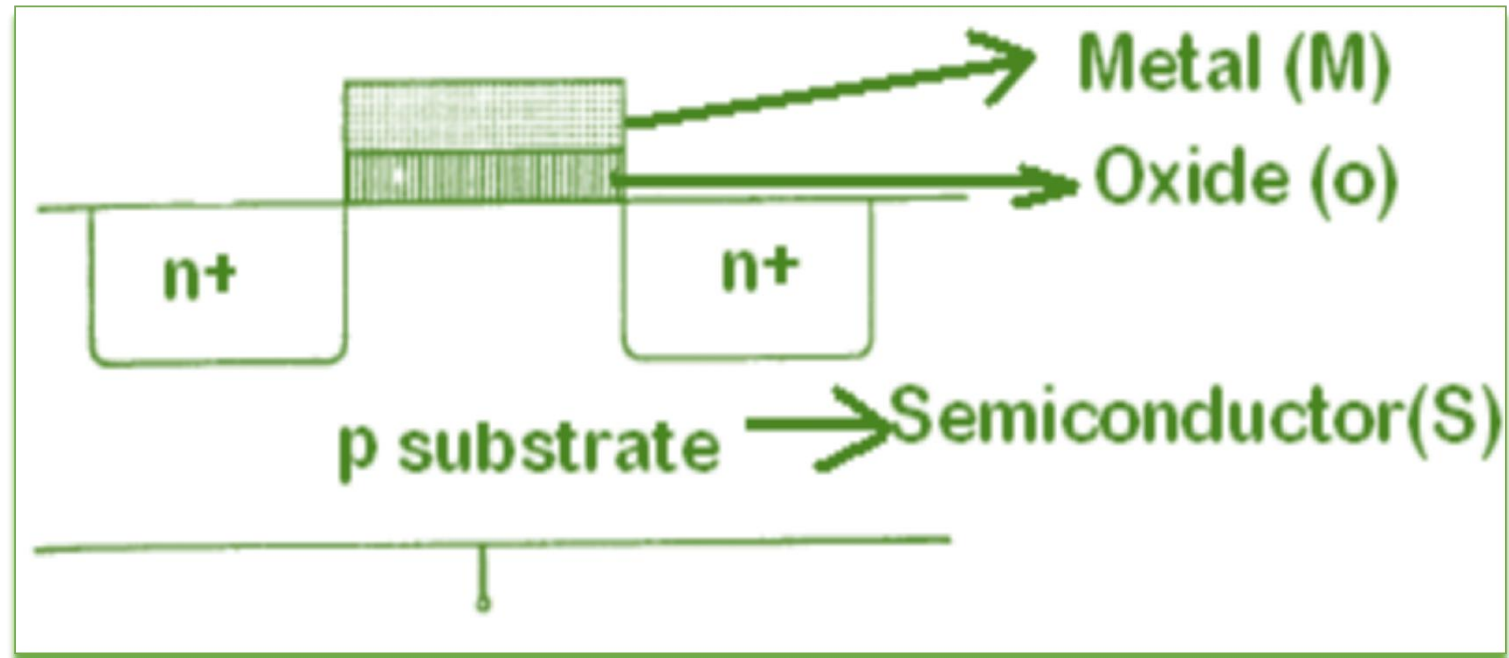
“The number of transistors embedded on the chip doubles after every one and a half years.”





WHY THE NAME MOS?

The structure consists of a layer of Metal (gate), a layer of oxide (SiO_2) and a layer of semiconductor





TWO MODE TRANSISTOR ACTION

In **Enhancement mode transistor channel** $\rightarrow +V_g$ **NMOS and PMOS enhancement transistors.**

In **Depletion mode transistor channel** $\rightarrow -V_g$
NMOS depletion mode transistors.

Example: Water tap












ACTIVITY




SOLVE IF YOU CAN

3	2	=	7
5	4	=	23
7	6	=	47
9	8	=	79
10	9	=	?

 +  +  = **60**

 +  = **26**

 +  = **15**

 +  ×  = **???**



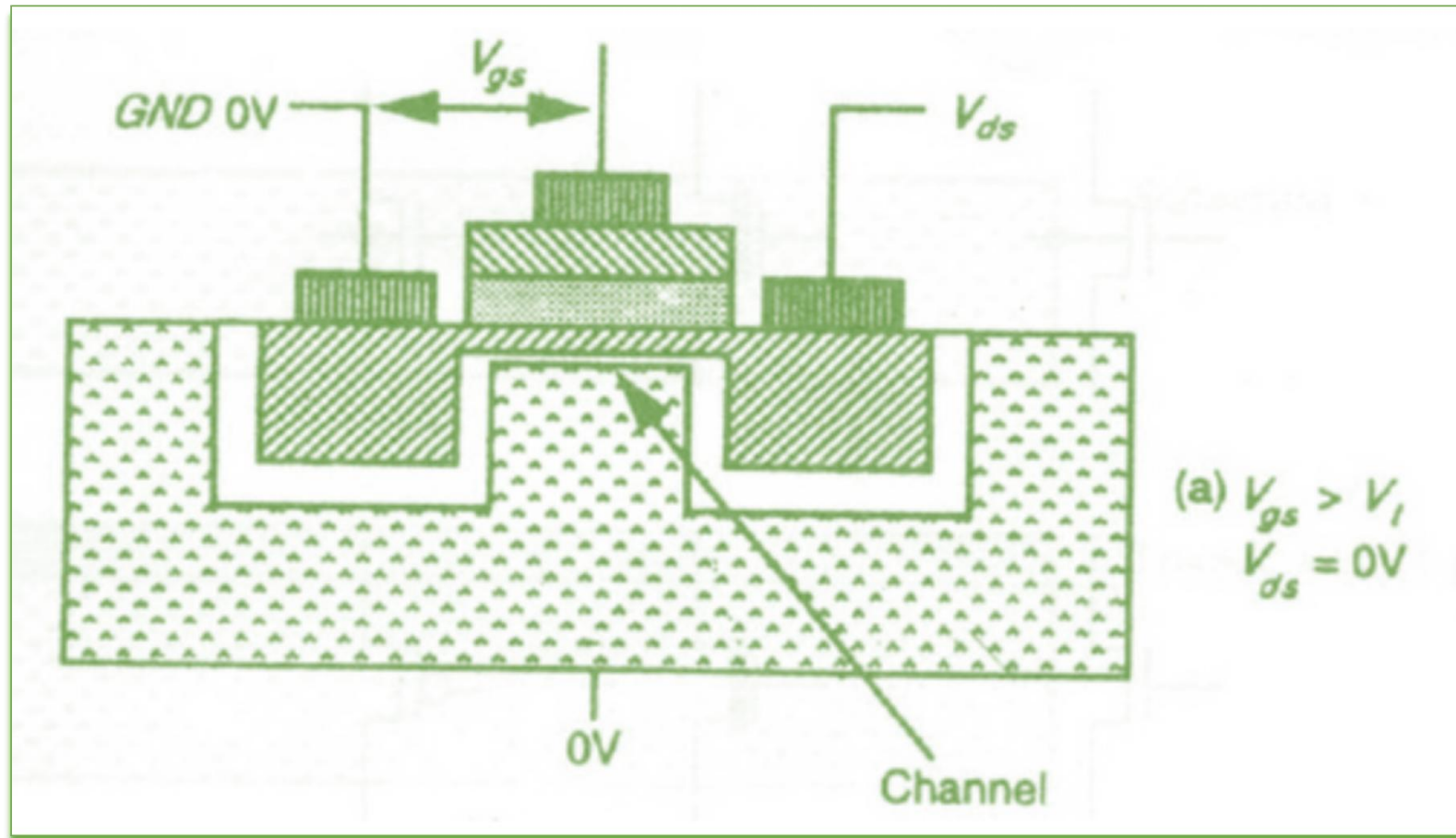
ENHANCEMENT MODE, DEPLETION MODE TRANSISTOR ACTION

Mode transistor	Gate Voltage	Channel	ON/OFF
N-MOS-enhancement	Positive	Electrons	ON
P-MOS-enhancement	Negative	Holes	ON, $V_t=0.2$ $V_{dd}=1$ or 5 V,
N-MOS - depletion	$-V$ b/w G & S	implanted	ON, $V_{gs}=0$

$\mu_n=2.5\mu_p \rightarrow$ nMOS is speed (pMOS is more R')
 $V_{td} < -0.8 V_{dd}$

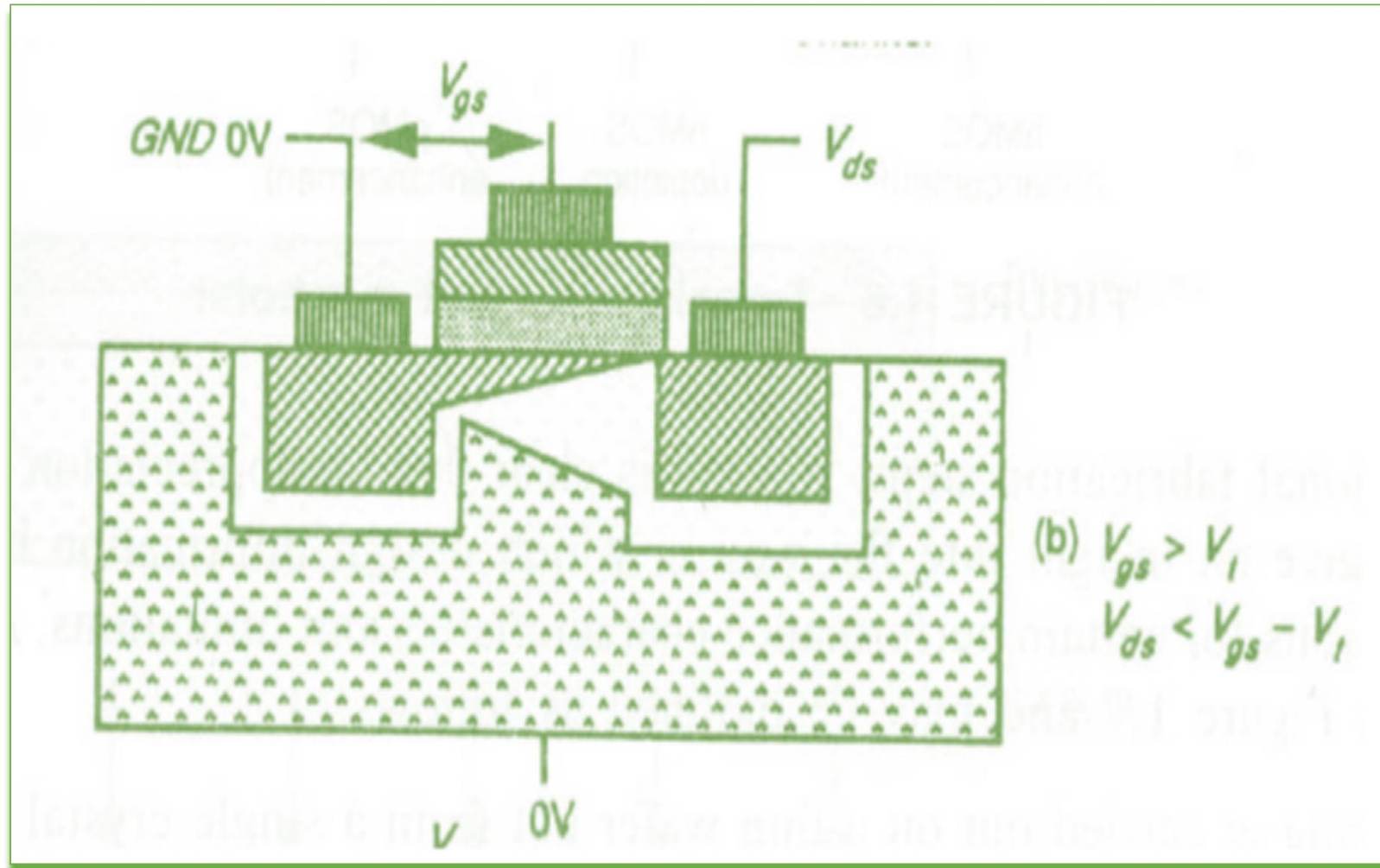


A) ENHANCEMENT MODE NO CURRENT FLOWS



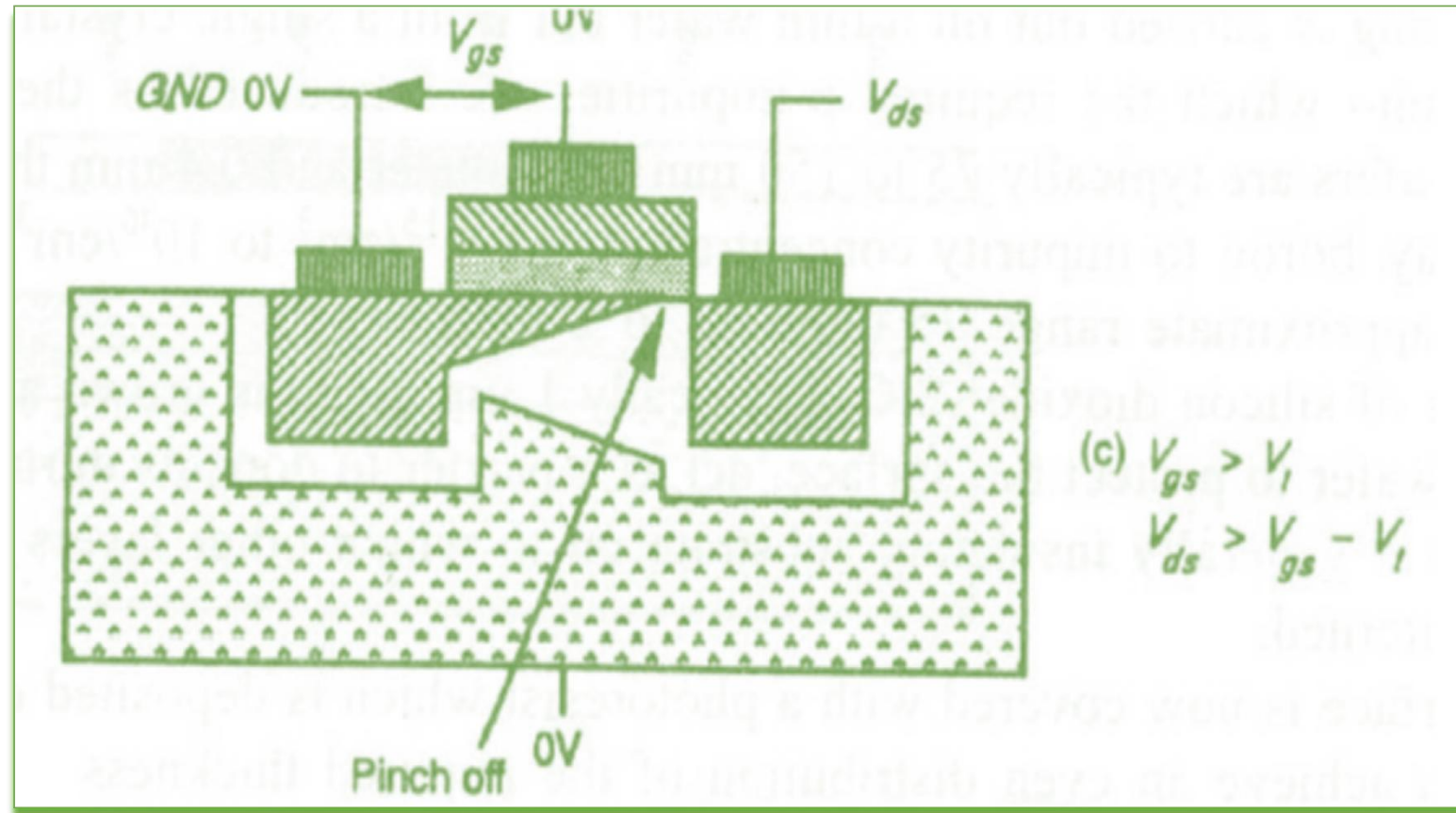


B) NON SATURATION



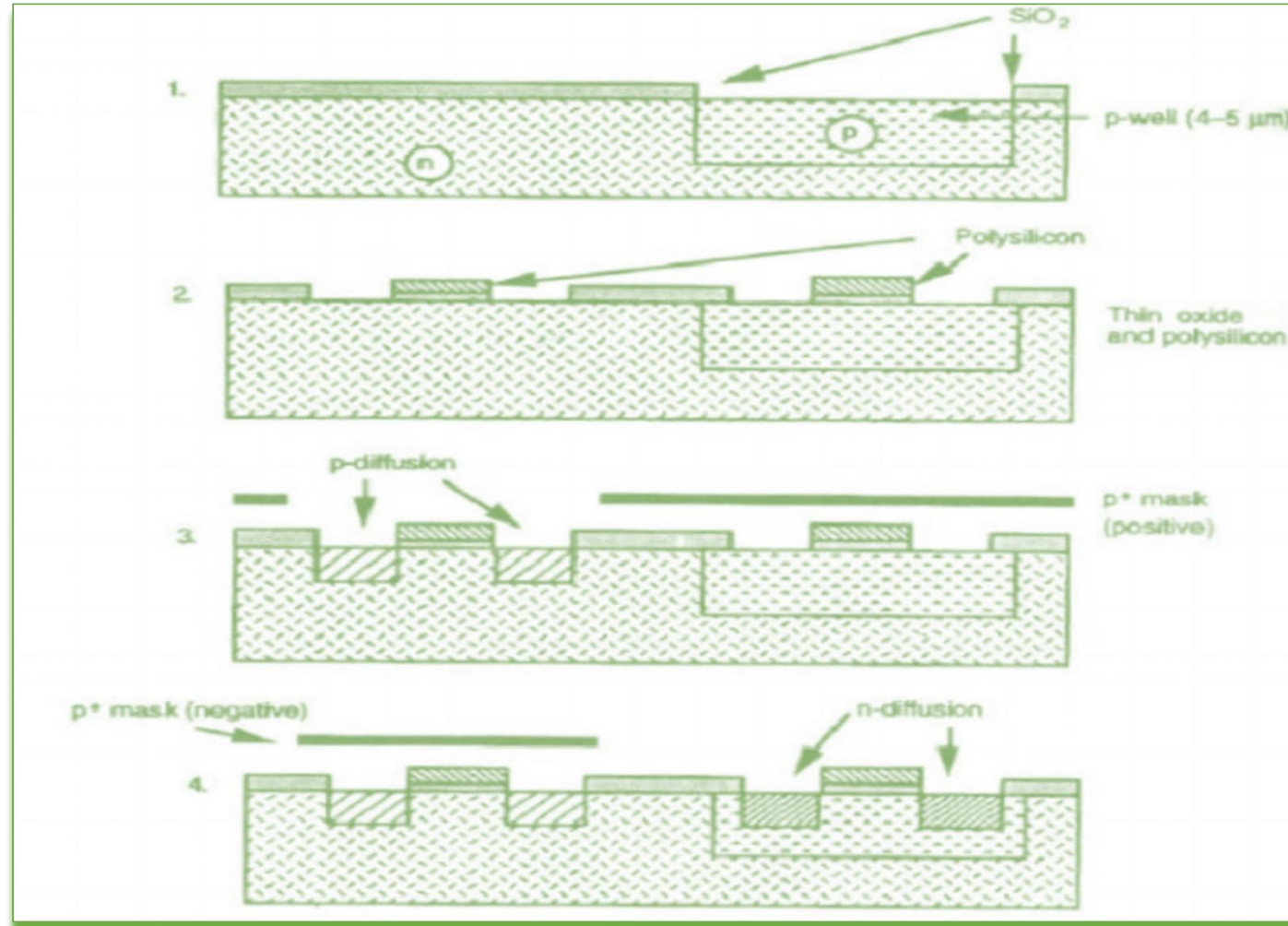


C) SATURATION-CONSTANT CURRENT





P-WELL PROCESS-MASKS LEVELS





P-WELL PROCESS-MASKS LEVELS

- 1-p-well diffusion defined
- 2-defines thinox, those areas where the thickox is stripped & thinox grown to accomodate p & n transistor & wires
- 3-pattern poly silicon layer-CVD
- 4- P+ MASK(+) –define all p diffusion areas(anded with mask2)

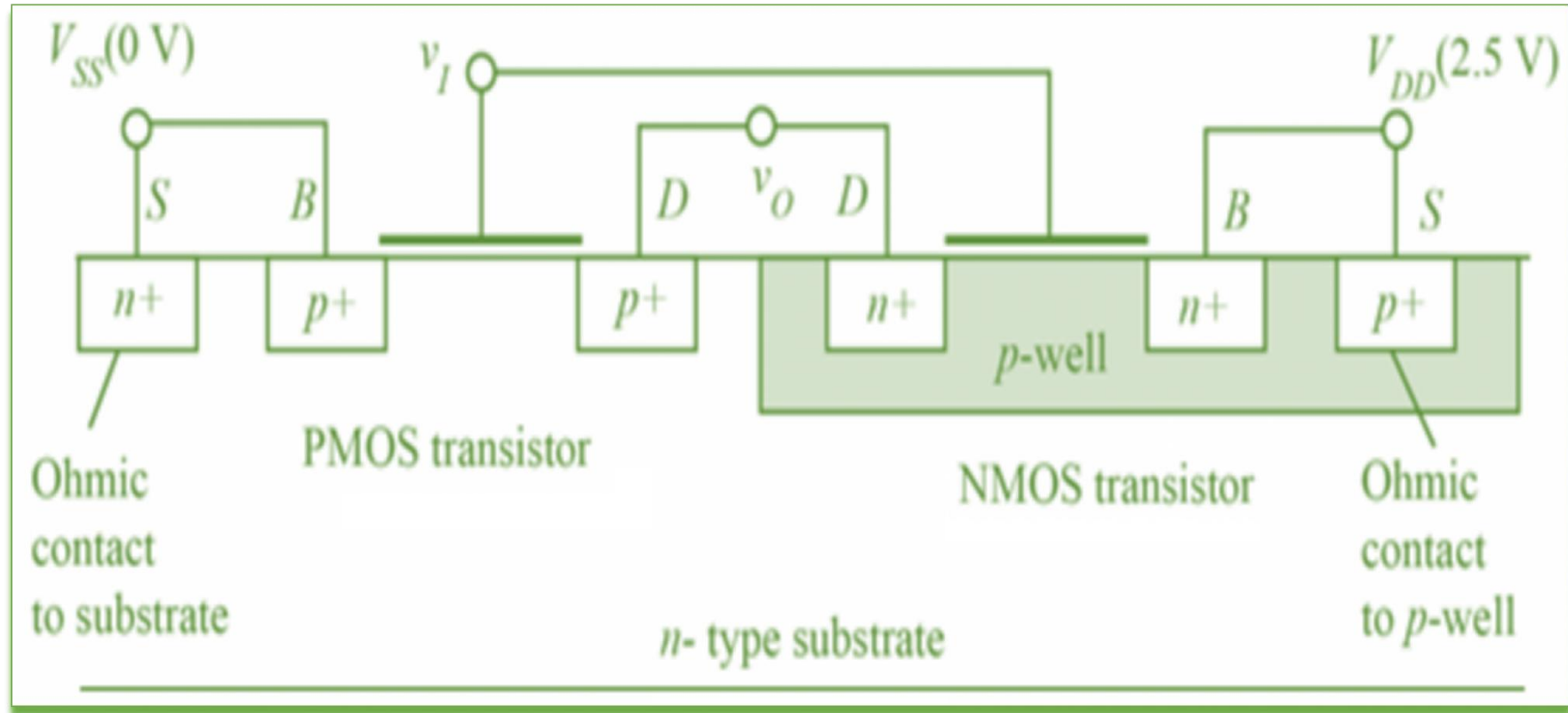


P-WELL PROCESS-MASKS LEVELS

- 5- P+ MASK(-) –define n-type diffusion (anded with mask2)
- 6-define contact cuts
- 7-define metal layer pattern
- 8-overall passivation (over glass)and opening for access to bonding pads



CMOS-P-WELL INVERTER





ASSESSMENT

1. $\mu_n = \dots \mu_p \rightarrow$ n / p MOS is speed

$$V_{td} < \dots V_{dd}$$

2. p-well Mask levels—1,3,5,7----?

3. p-well Mask levels—2,4,6,8----?

4. Non Saturation $V_{ds} = ??$

5. Define Pinch off?



SUMMARY

THANK YOU...