SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

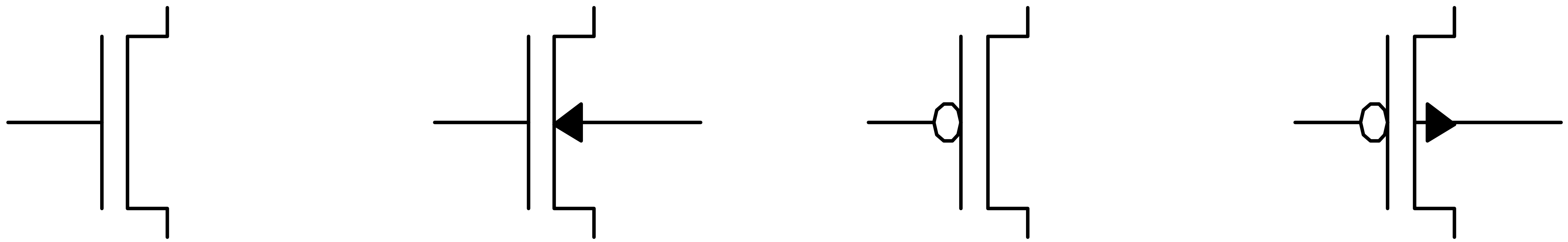
TOPIC 4 –MOS IV CHARACTERISTICS

OUTLINE

- INTRODUCTION
- MOS CAPACITOR
- TERMINAL VOLTAGES
- NMOS CUTOFF
- NMOS LINEAR
- NMOS SATURATION
- I-V CHARACTERISTICS
- CARRIER VELOCITY
- ACTIVITY
- NMOS & PMOS I-V PLOTS
- EXAMPLES
- ASSESSMENT
- SUMMARY

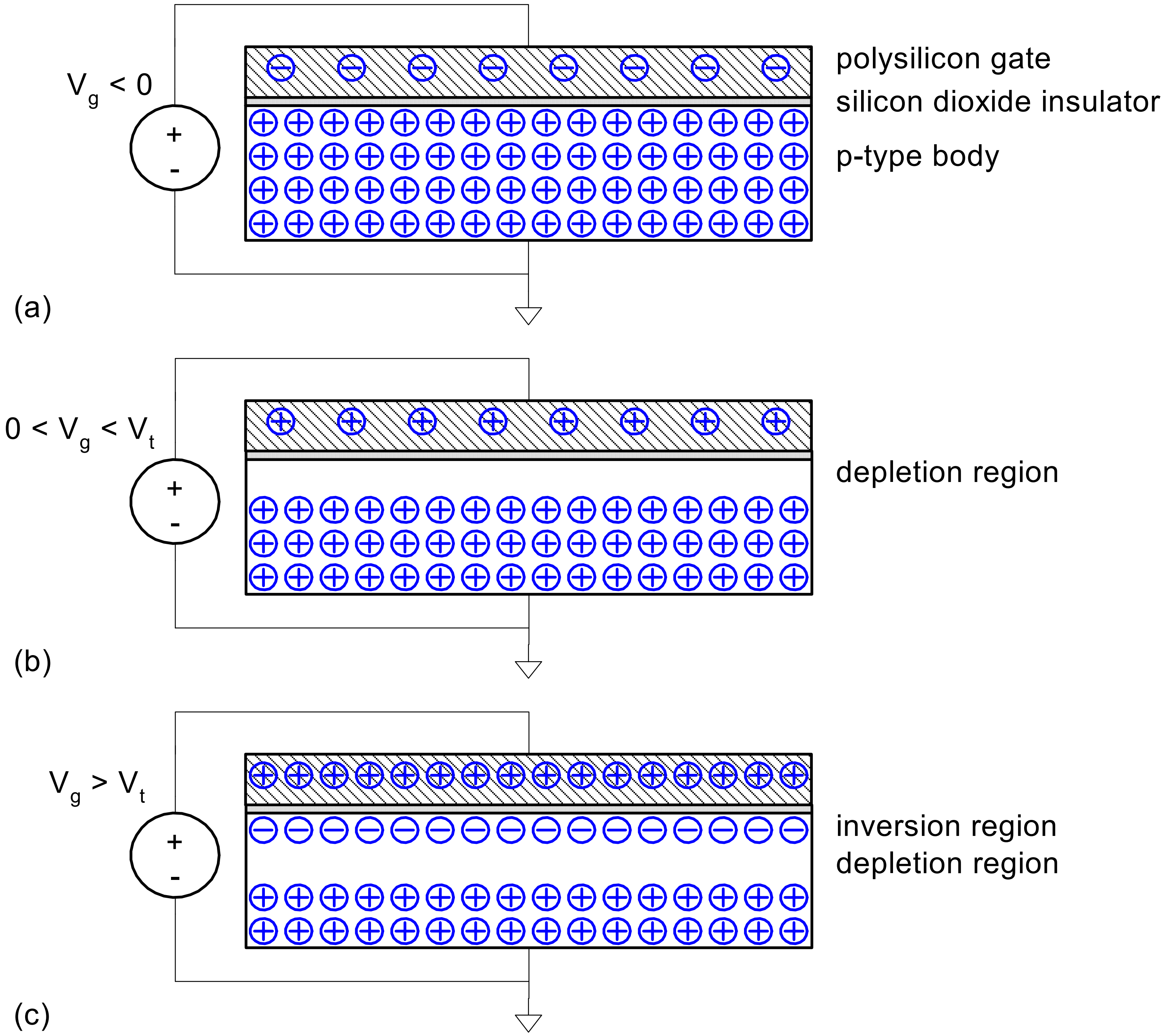
INTRODUCTION

- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - I = C (DV/Dt) -> Dt = (C/I) DV
  - Capacitance and current determine speed
- Also explore what a “degraded level” really means



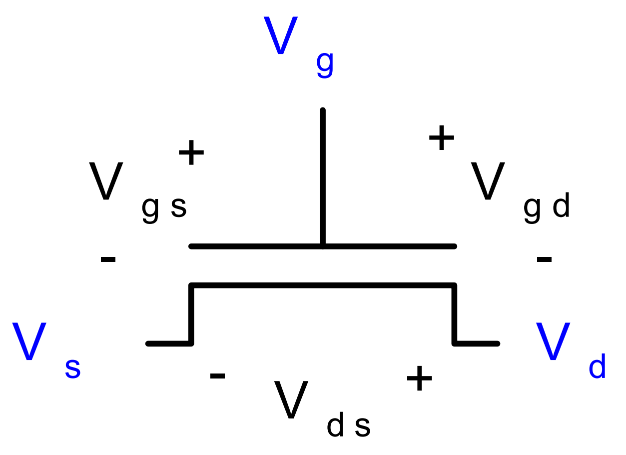
MOS CAPACITOR

- Gate and body form MOS capacitor
- Operating modes
  - –Accumulation
  - –Depletion
  - –Inversion



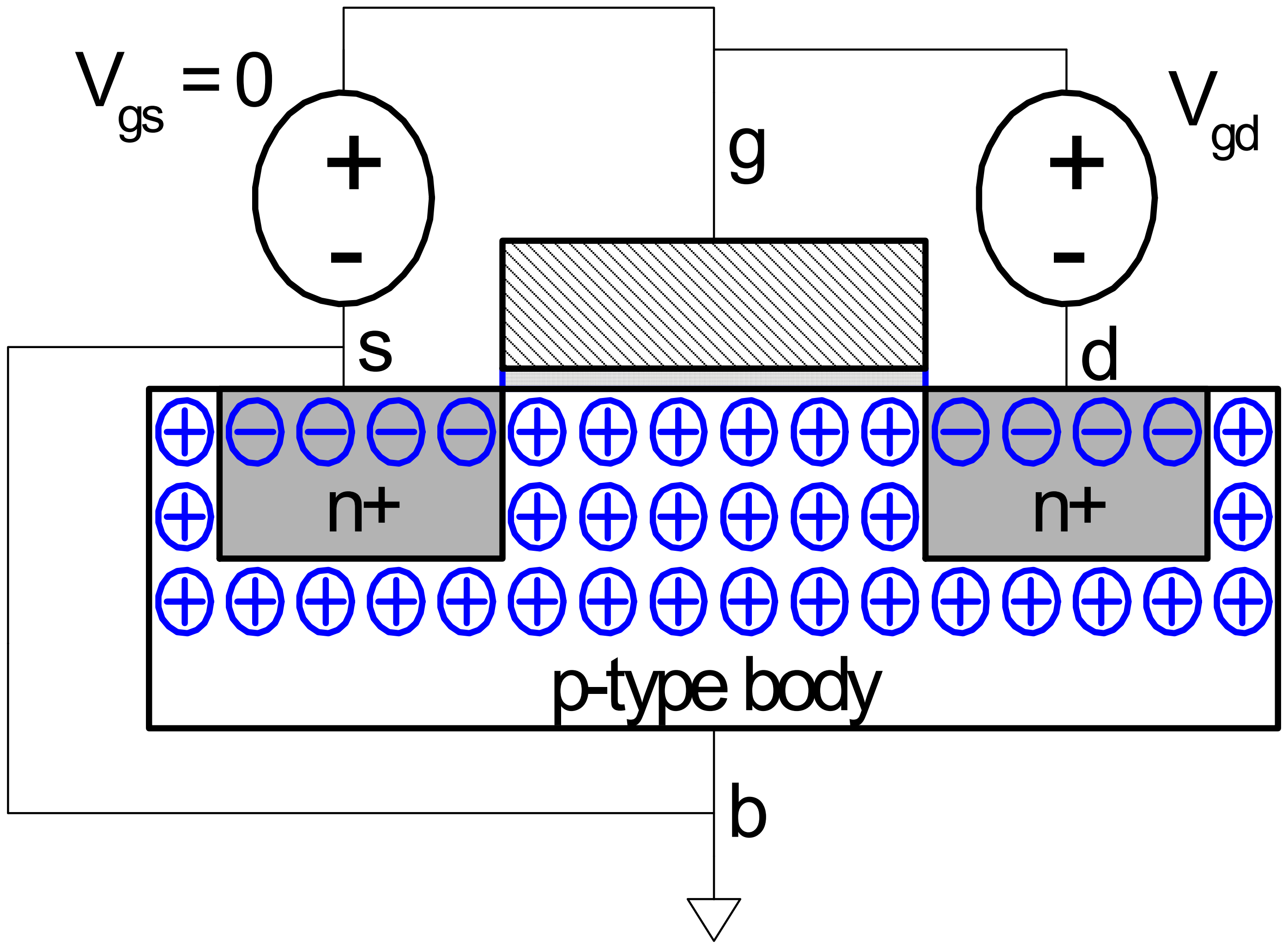
TERMINAL VOLTAGES

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage ,Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - Cutoff
  - Linear
  - Saturation



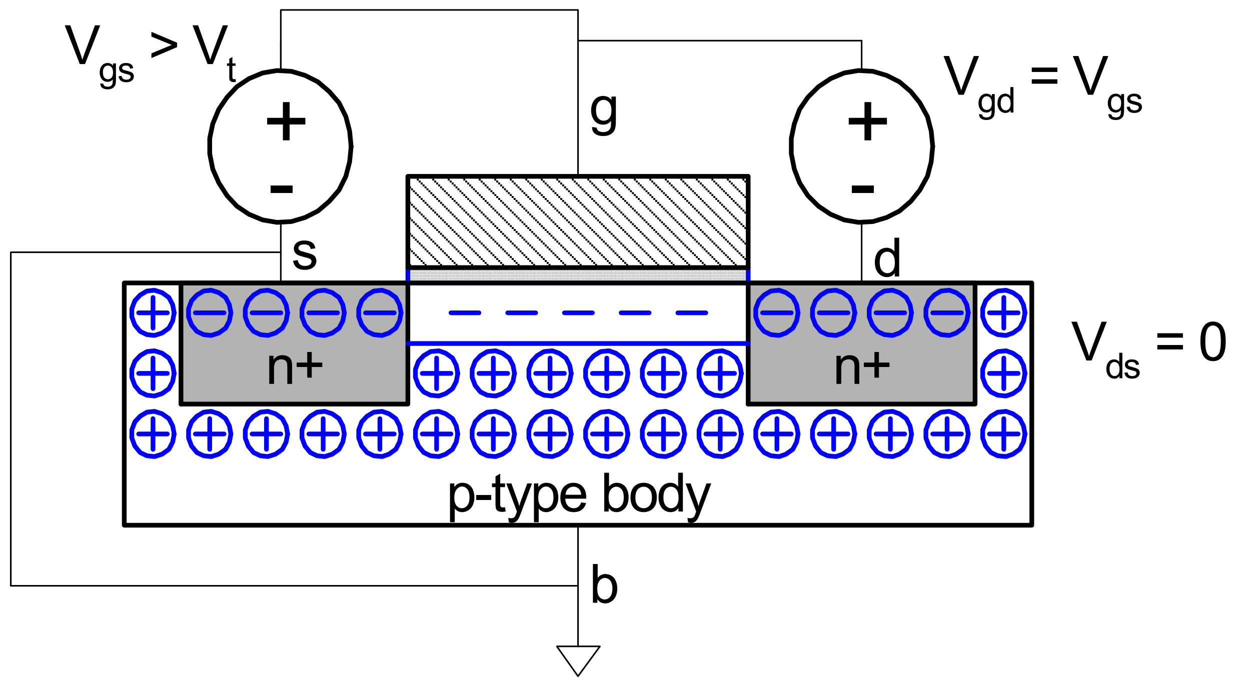
NMOS CUTOFF

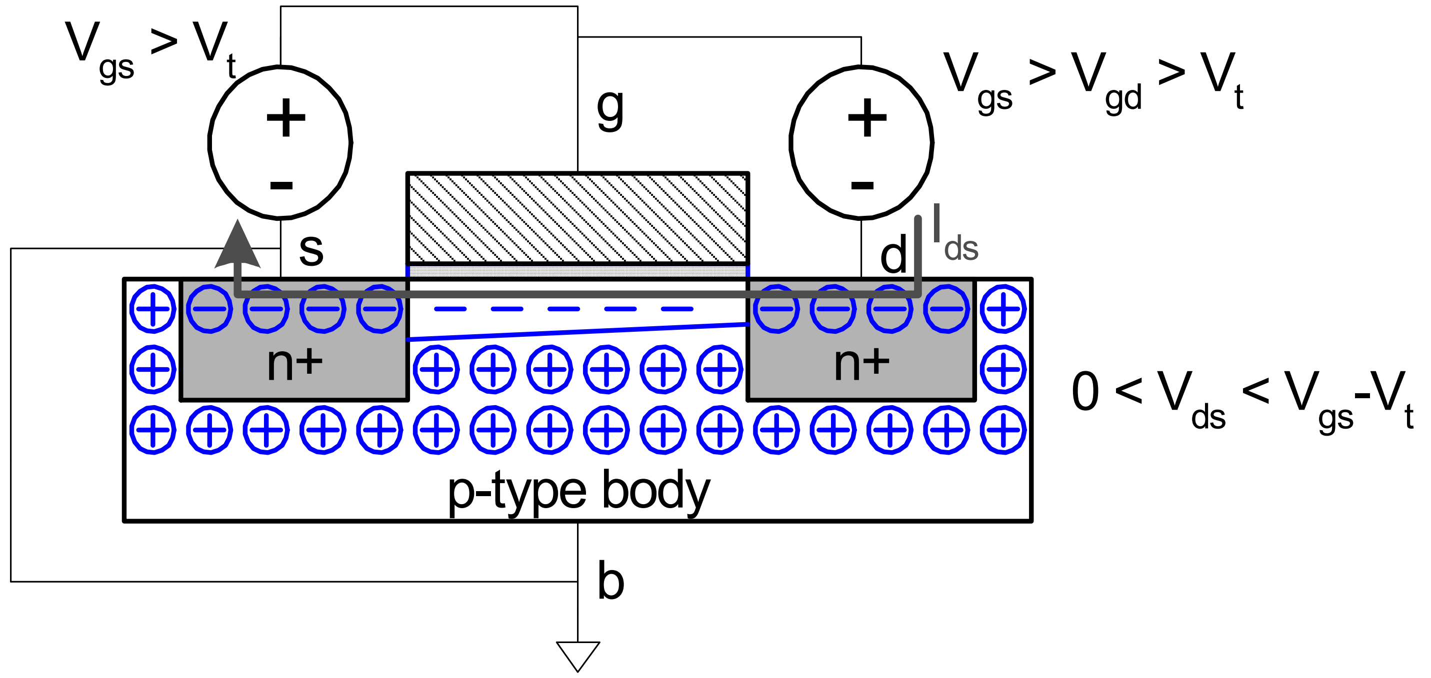
- No channel
- $I_{ds} = 0$



NMOS LINEAR

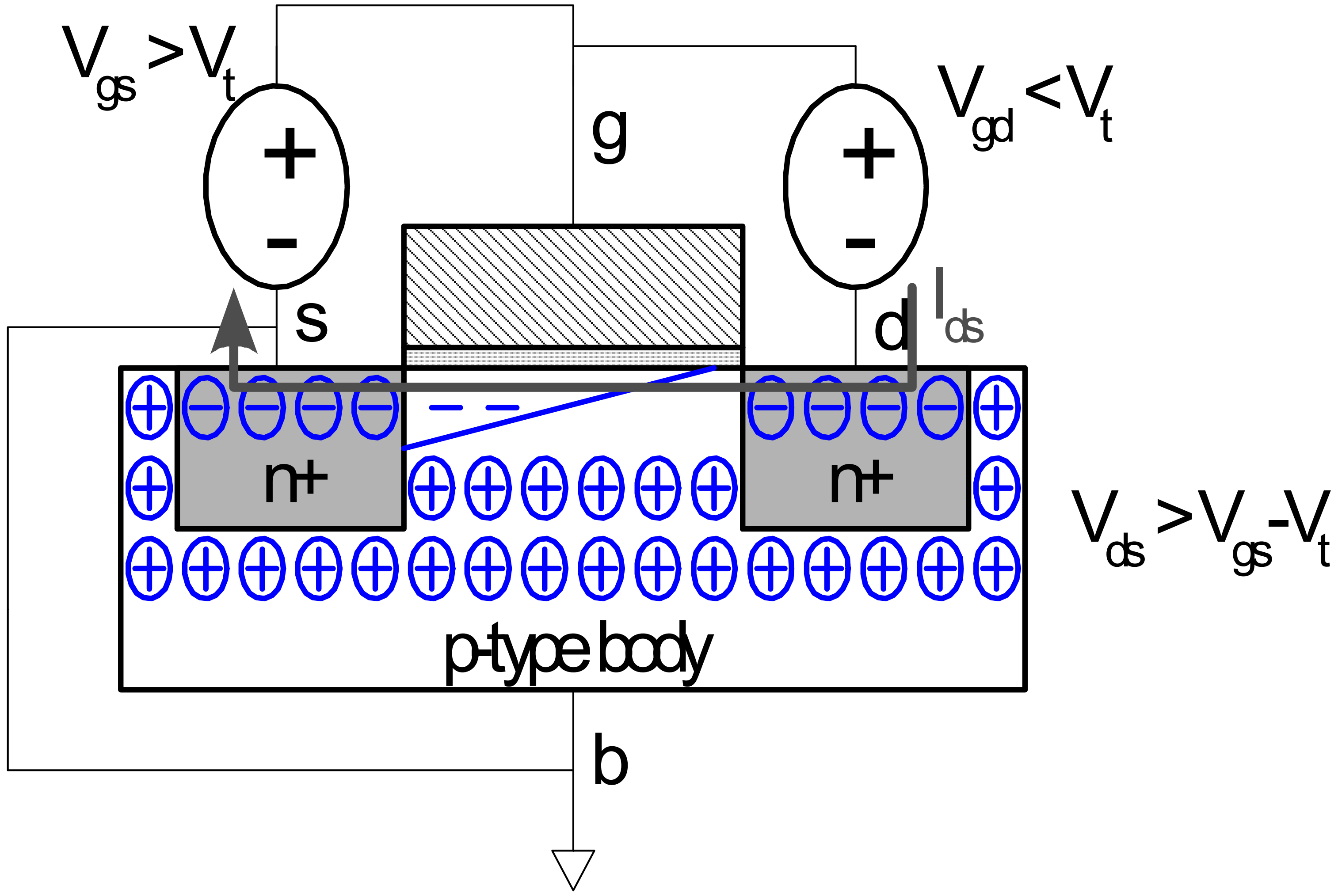
- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor





NMOS SATURATION

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current saturates
- Similar to current source



I-V CHARACTERISTICS

What is I & V?????

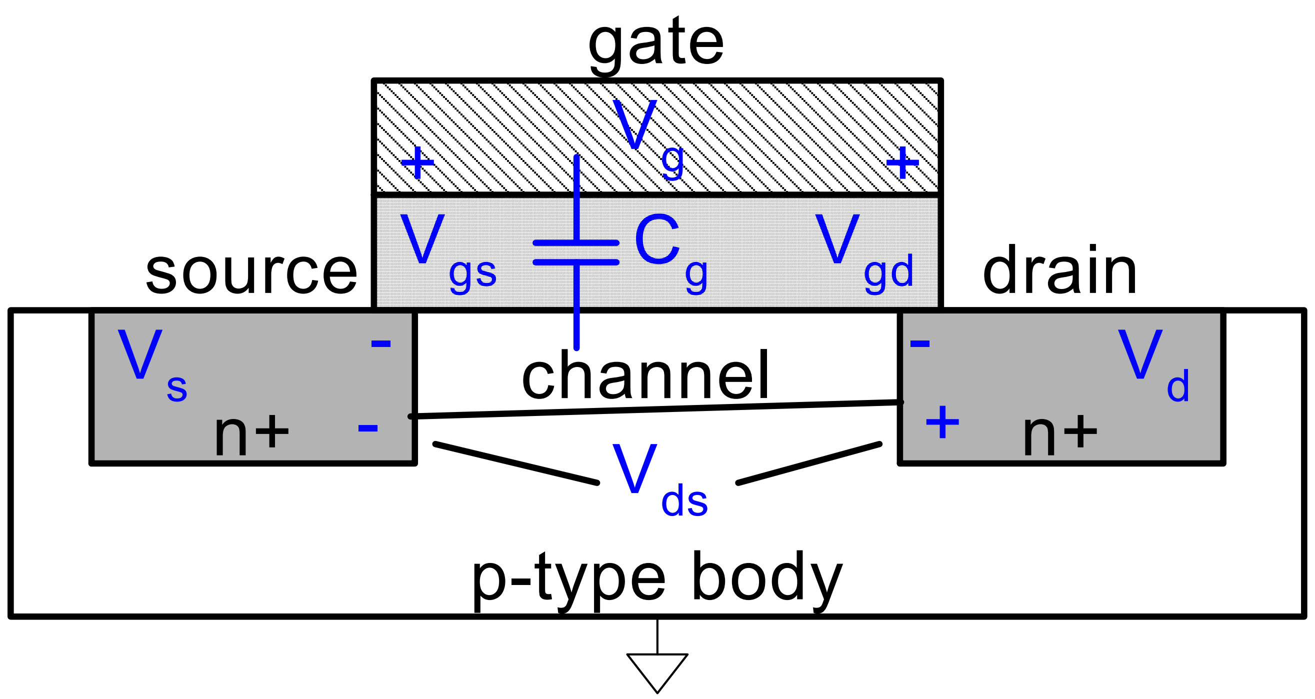
In Linear region, I_{ds} depends on

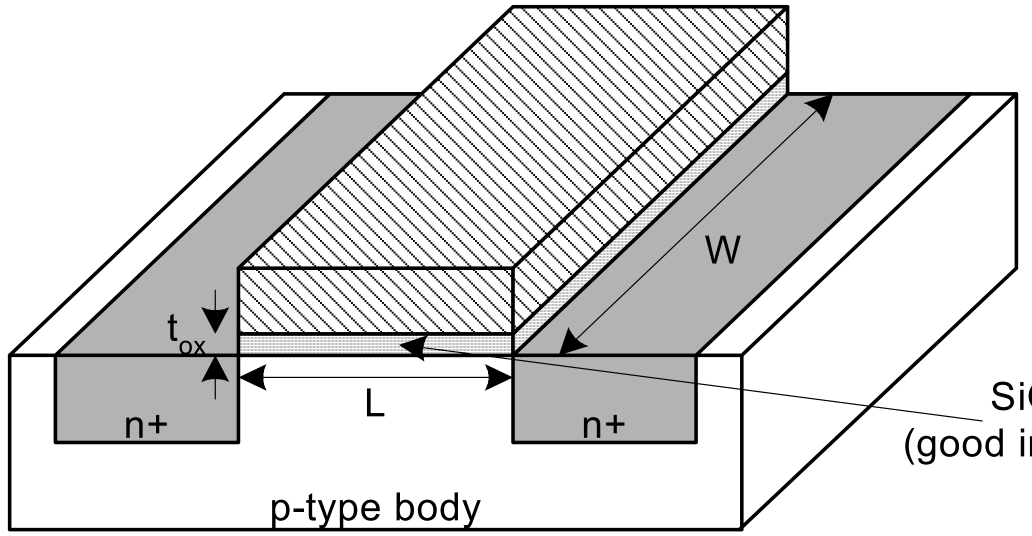
How much charge is in the channel?

How fast is the charge moving?

CHANNEL CHARGE

- MOS structure looks like parallel plate capacitor while operating in inversion
  - –Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = e_{ox}WL/t_{ox} = C_{ox}WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

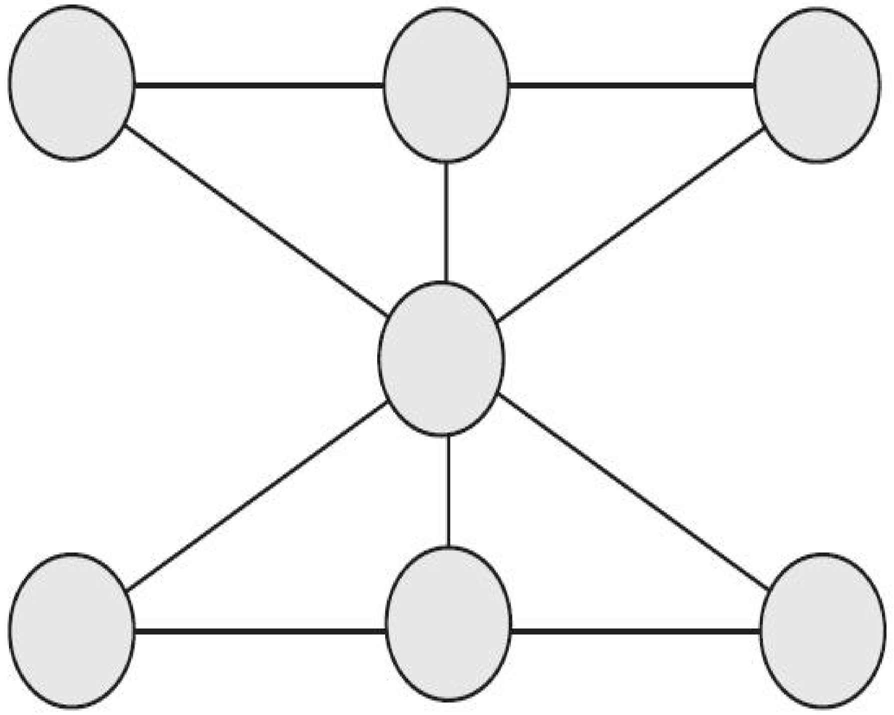




CARRIER VELOCITY & ACTIVITY

- Charge is carried by e-
- Carrier velocity v proportional to lateral E-field between source and drain
- $v = \text{m}E$ m called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

•Can you put the numbers 1 to 7 In the circles so that every line adds up to 12? You can use each number only once.



NMOS LINEAR I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time t each carrier takes to cross

$$
\begin{aligned}
I_{ds} &= \frac{Q_{\text{channel}}}{t} \\
&= \mu C_{\text{ox}} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \\
&= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}
\end{aligned}
$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

NMOS SATURATION I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

PMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility m_p is determined by holes
  - Typically 2-3x lower than that of electrons m_n
  - 120 $cm^2/V{*}s$ in AMI 0.6 mm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $m_n / m_p = 2$

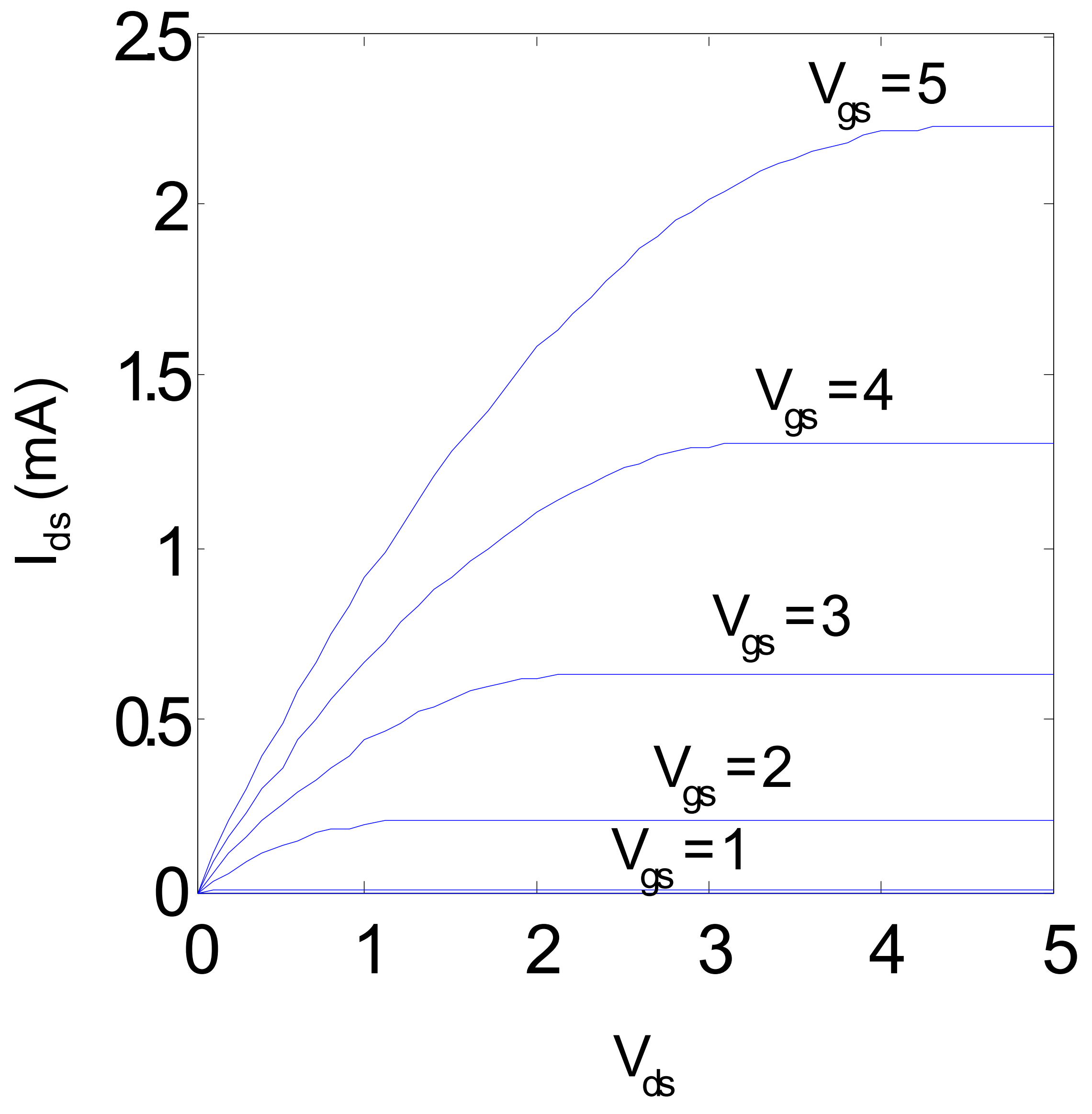
NMOS I-V SUMMARY

- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - \dfrac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \dfrac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

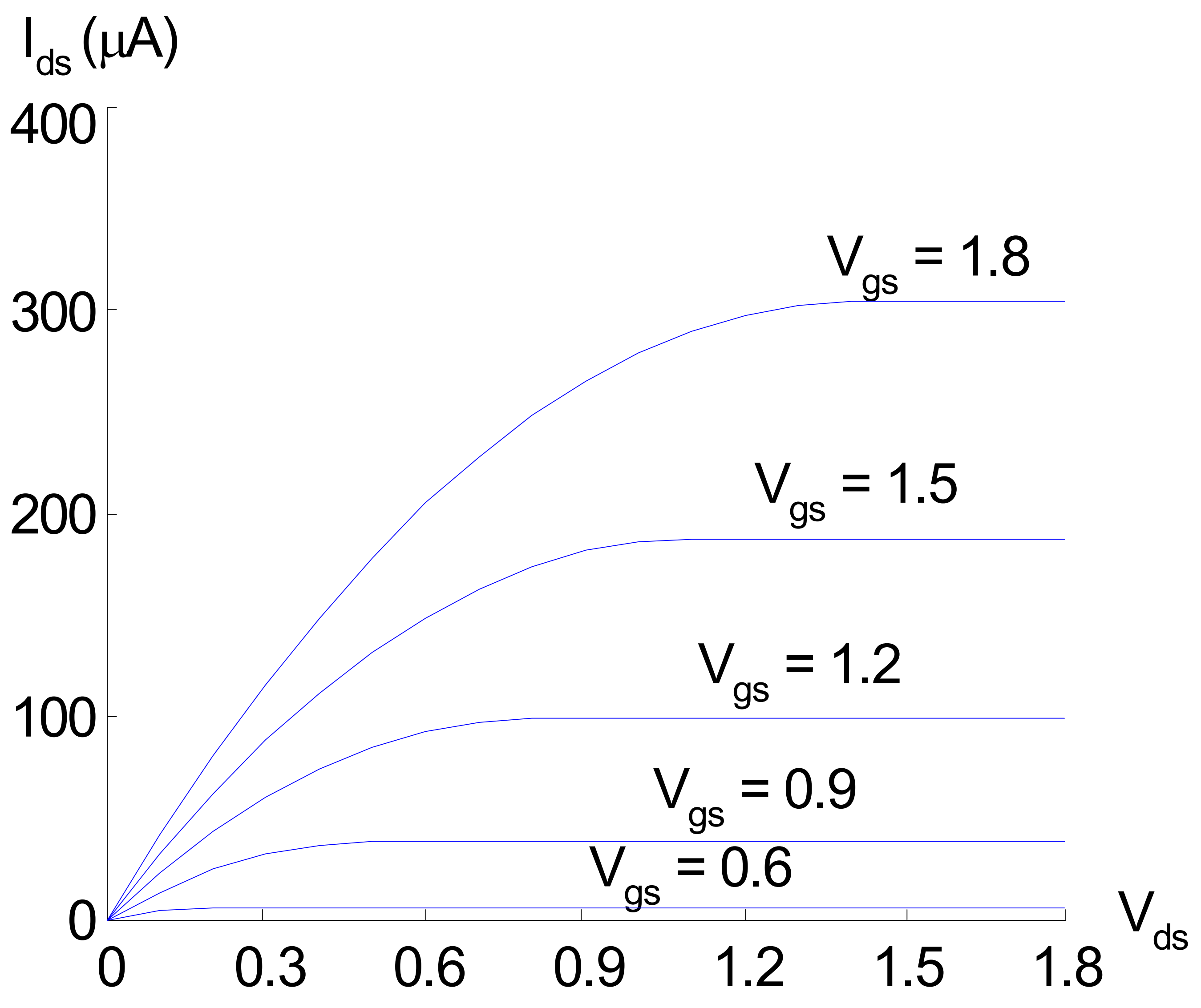
EXAMPLE

- We will be using a 0.6 mm process for your project
  - From AMI Semiconductor
  - t_{ox} = 100 Å
  - m = 350 cm²/V*s
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 l



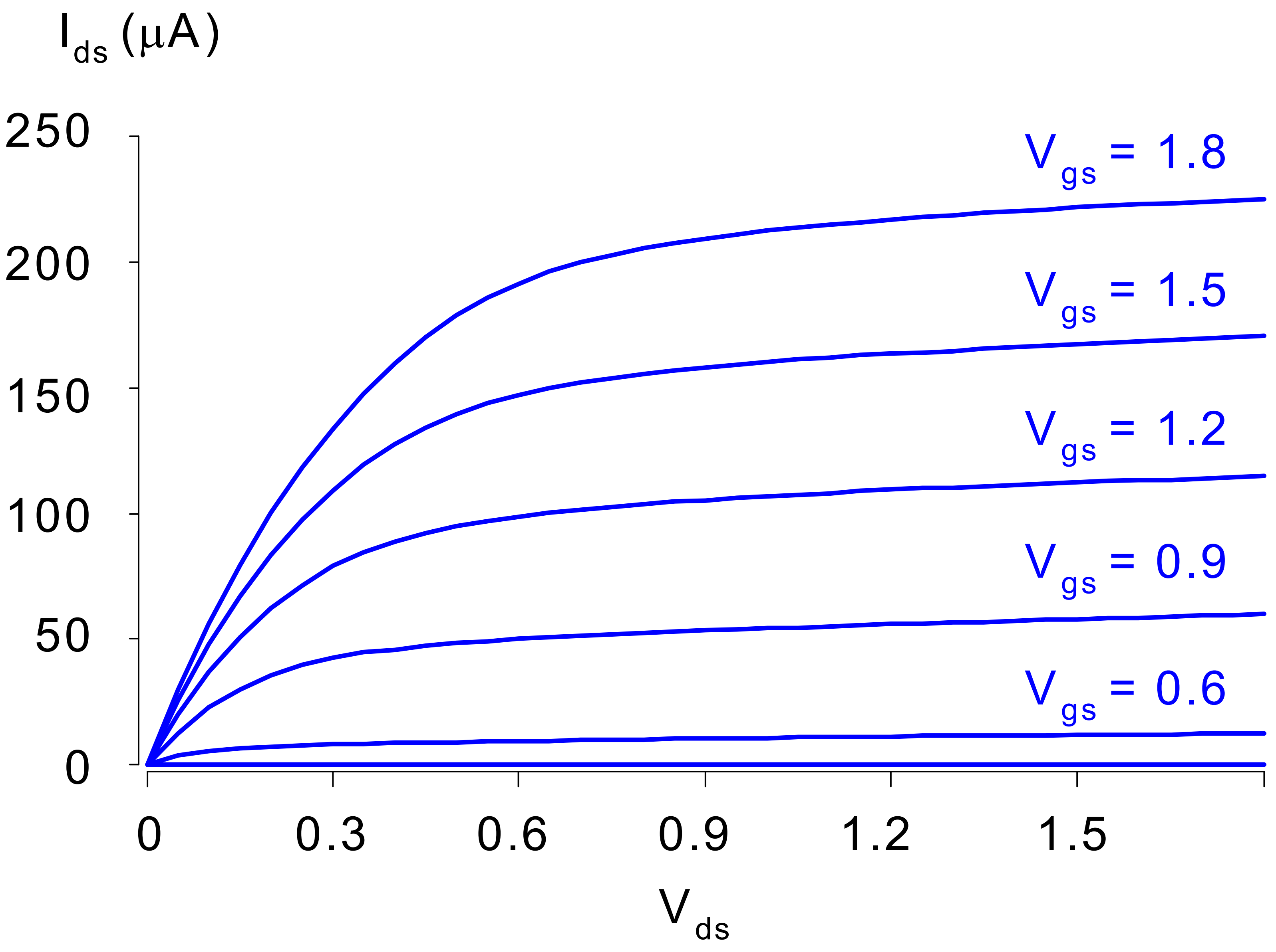
IDEAL NMOS I-V PLOT

- 180 nm TSMC process
- Ideal Models
  - b = 155(W/L) mA/V²
  - $V_t = 0.4$ V
  - $V_{DD} = 1.8$ V



SIMULATED NMOS I-V PLOT

- 180 nm TSMC process
- BSIM 3v3 SPICE models
- What differs?
  - ➢Less ON current
  - ➢No square law
  - ➢Current increases
  - ➢ in saturation



ASSESSMENT

1.Compare Accumulation,Depletion,Inversion modes

2. Write the I_{ds} equations for three modes in Shockley 1st order transistor models

3.Draw pMOS I-V plot

SUMMARY & THANK YOU