SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

11/24/2023

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC 2 &3 –Pass transistor Logic, Transmission gates

OUTLINE

- A Brief History
- CMOS Gate Design
- Pass Transistors
- Transmission Gate logic
- Activity
- Assessment
- Summary

A Brief History

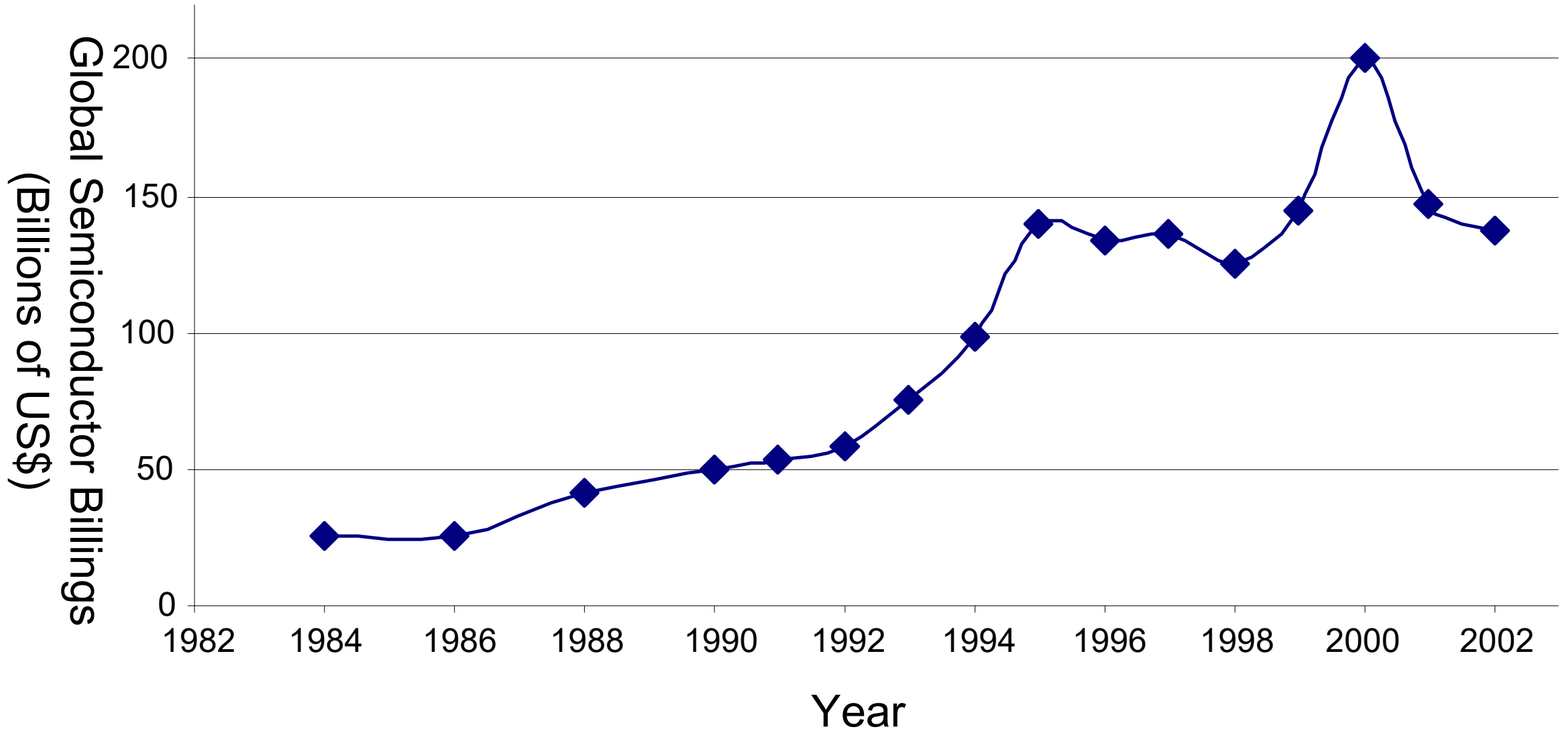
1958: First integrated circuit

- Flip-flop using two transistors
- Built by Jack Kilby at Texas Instruments

2003-Intel Pentium 4 mprocessor (55 million transistors)

512 Mbit DRAM (> 0.5 billion transistors) miniaturization of transistors Smaller is cheaper, faster, lower in power! Revolutionary effects on society

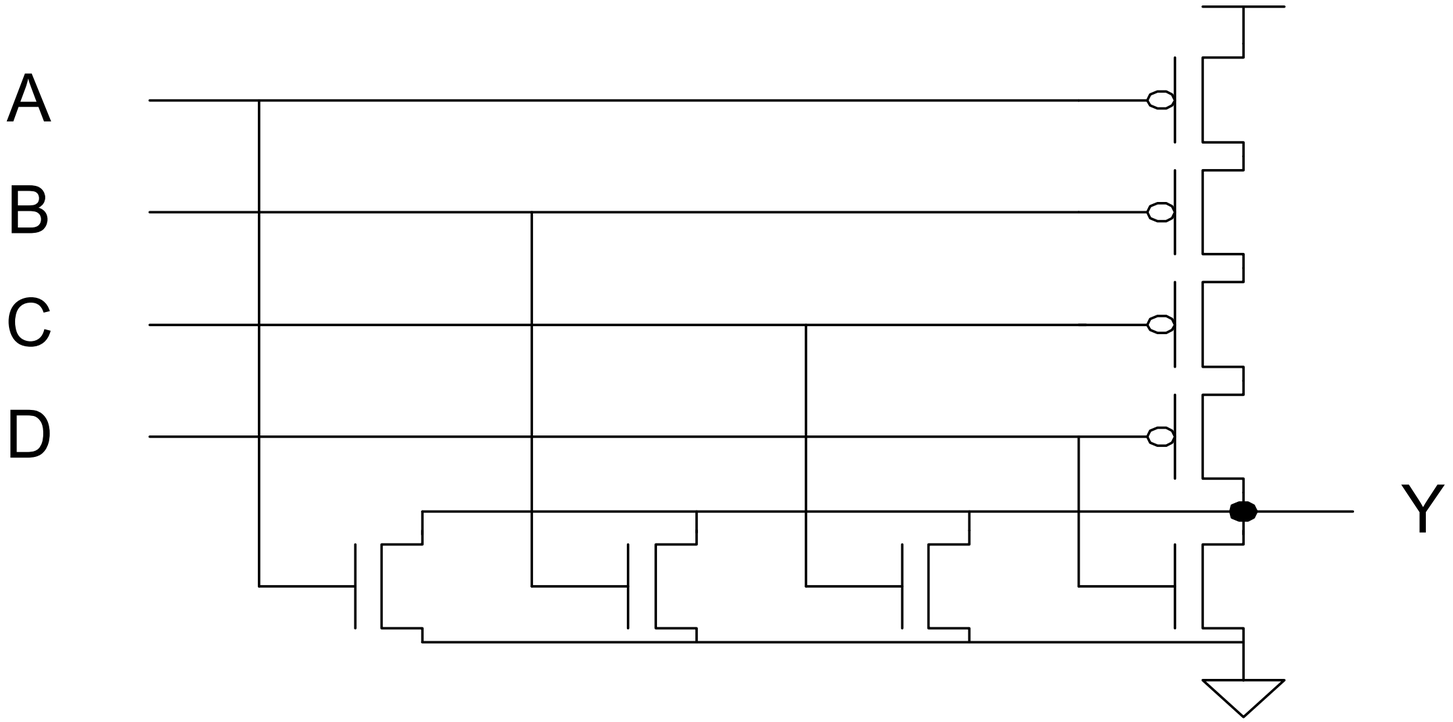
Annual Sales



Transistor Types

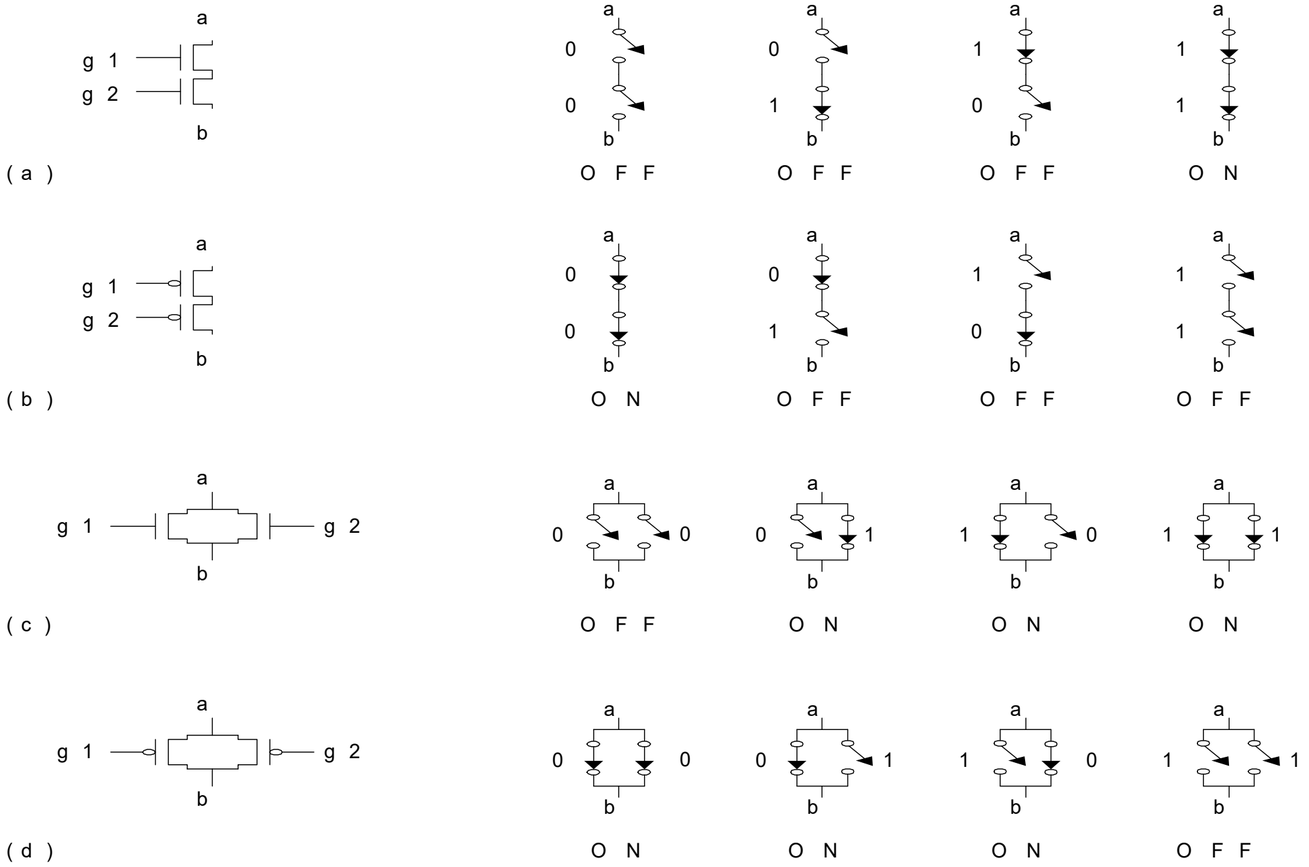
- **Bipolar transistors**
  - npn or pnp silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - Base currents limit integration density
- **Metal Oxide Semiconductor Field Effect Transistors**
  - nMOS and pMOS MOSFETS
  - Voltage applied to insulated gate controls current between source and drain
  - Low power allows very high integration

CMOS Gate Design-4 input NOR



Series and Parallel Connections

- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON



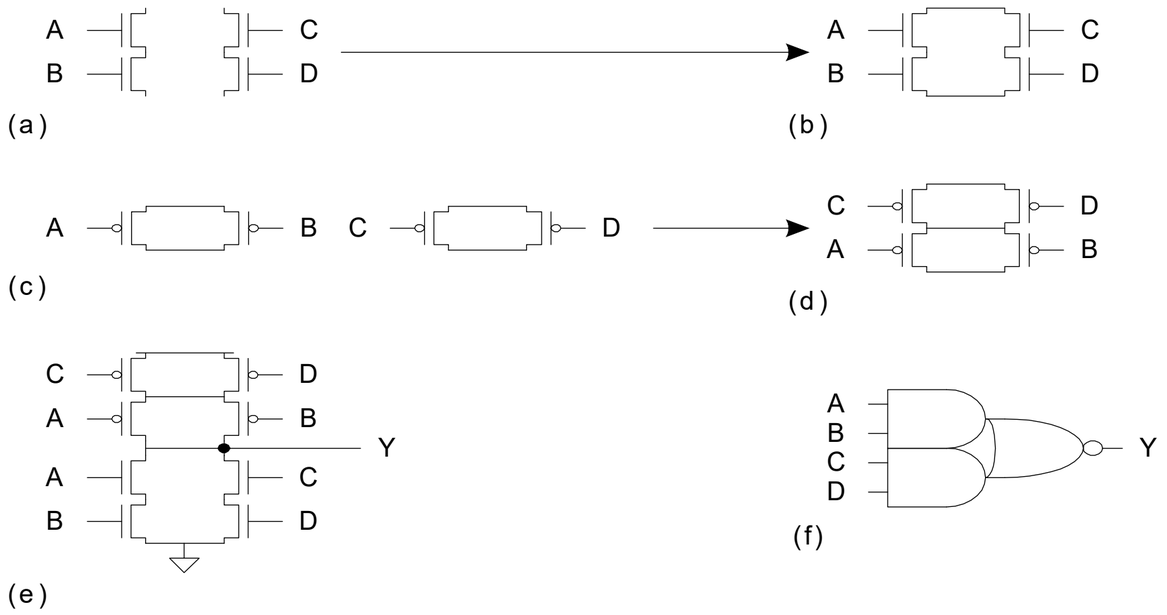
Conduction Complement

- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate- .ns—n-MOS Series—pMOS parallel
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS

- Rule of Conduction Complements
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel

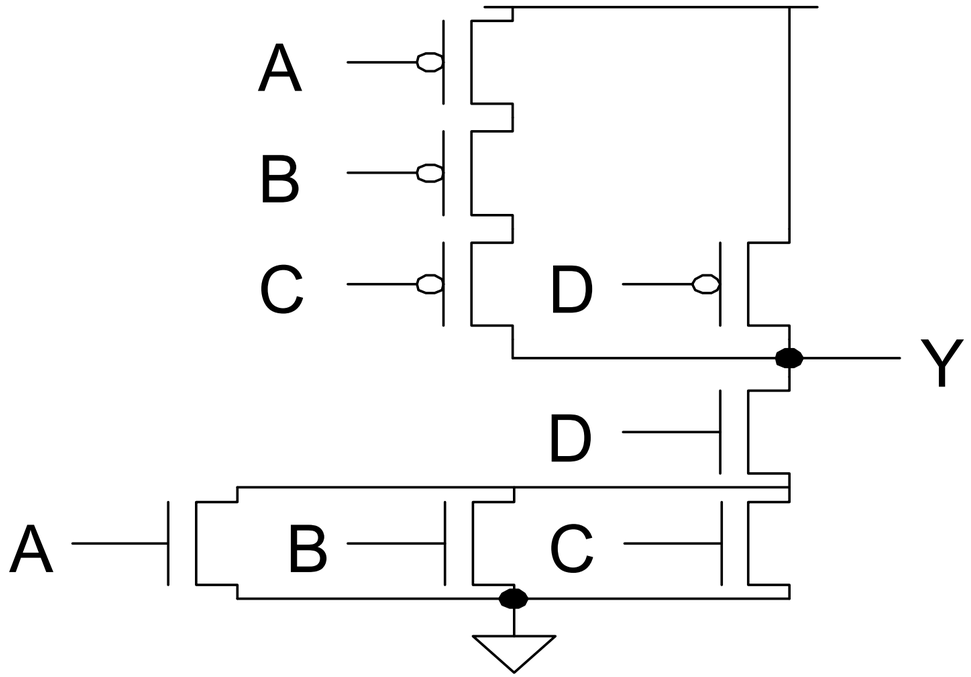
Compound Gates

- Compound gates can do any inverting function
- Ex: $Y = \overline{A\ B + C\ D}$ (AND-AND-OR-INVERT, AOI22)



Example: O3AI

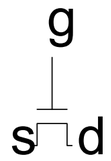
$$Y = \overline{(A + B + C)\ D}$$



Strength of Signal

How close it approximates ideal voltage source

V_{DD} and GND rails are strongest 1 and 0

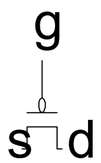


•nMOS pass strong 0

But degraded or weak 1

•pMOS pass strong 1

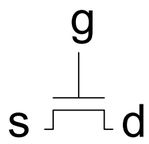
But degraded or weak 0

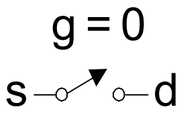


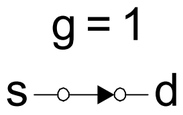
Thus nMOS are best for pull-down network

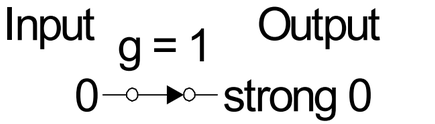
Pass Transistors

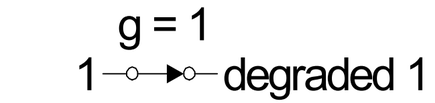
Transistors can be used as switches

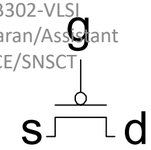


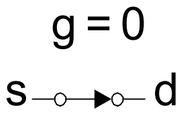


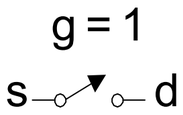


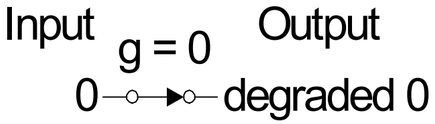






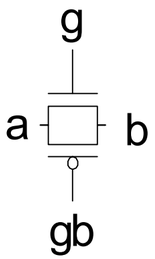


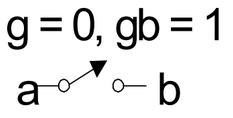


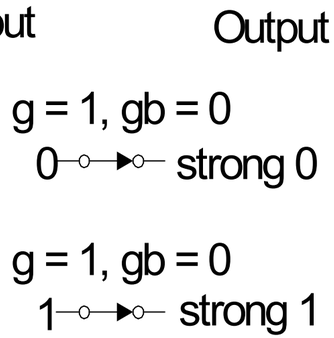


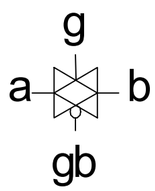
Transmission Gates

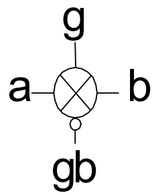
- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

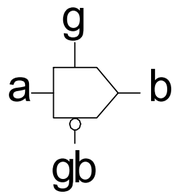








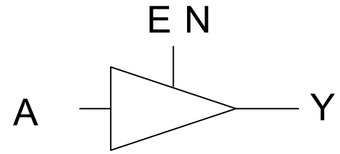


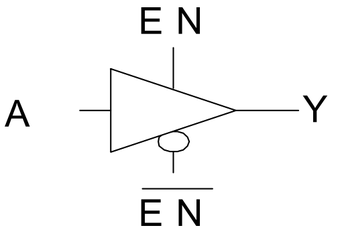


Tristates

- Tristate buffer produces Z when not enabled

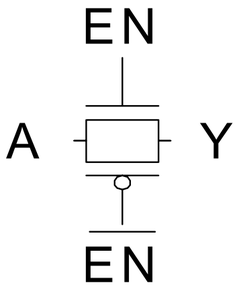
EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1





Non restoring Tristate

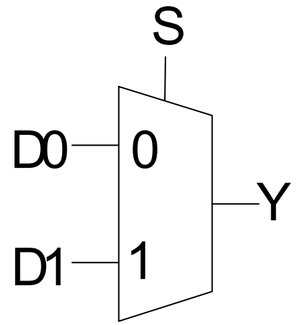
- Transmission gate acts as tristate buffer
  - Only two transistors
  - But non restoring
    - Noise on A is passed on to Y



Multiplexers

- 2:1 multiplexer chooses between two inputs

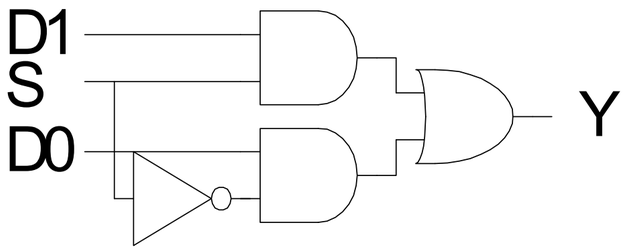
S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

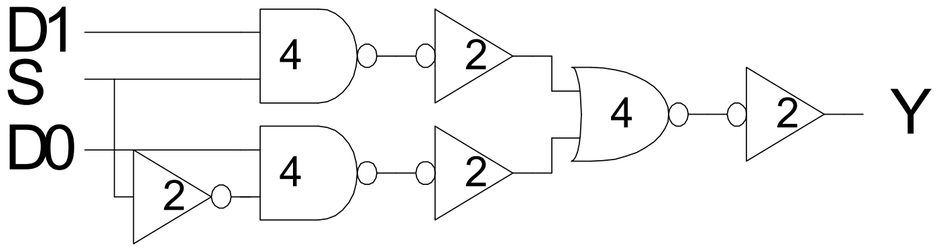


Gate-Level Mux Design

$Y = SD_1 + \overline{S}D_0$ (too many transistors)

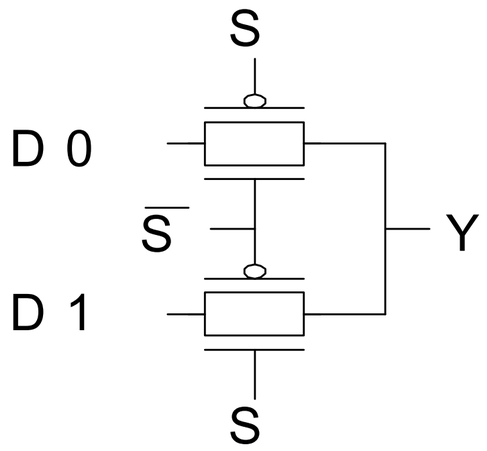
How many transistors are needed? 20





Transmission Gate Mux

- Nonrestoring mux uses two transmission gates
  - Only 4 transistors



Assessment

How many transistors are needed to

make 2:1 Mux? ---

Draw 2:1 mux using TG

Draw 4:1 mux using TG

nMOS pass strong -------

But degraded or weak ------

pMOS pass strong -----

But degraded or weak ----------

Thus nMOS are best for pull-down network

THANK YOU

EXAMPLES OF COMBINATIONAL LOGIC/19ECB302-VLSI DESIGN/J.Prabakaran/Assistant Professor/ECE/SNSCT