SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB302–VLSI DESIGN

III YEAR/ V SEMESTER

11/24/2023

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC 4 & 5 –Pseudo nMOS logic & Domino Logic

OUTLINE

- Pseudo NMOS logic
  - Comparison of 3 Gates
  - Pseudo nMOS Design & power calculation
- Dynamic Logic
  - The Foot,LogicalEffort,Monotonocity problem
- Activity
- Domino Gates
  - Optimization ,Dual Rail
- Assessment
- Summary

Pseudo NMOS logic

- The inverter that uses a p-device pull-up or load that has its gate permanently ground.
- An n-device pull-down or driver is driven with the input signal. This roughly equivalent to use of a depletion load is **Nmos** technology and is thus called '**Pseudo-NMOS**'.
- This circuit is used in a variety of CMOS **logic** circuits

Pseudo NMOS logic – Advantage and Disadvantage

- The **advantage** of pseudo-NMOS logic are its high **speed** (especially, in large-fan-in NOR gates) and low transistor count.

- The **Disadvantage** On the negative side is the static **power** consumption of the pull-up transistor as well as the reduced output voltage swing and gain, which makes the gate more susceptible to noise.

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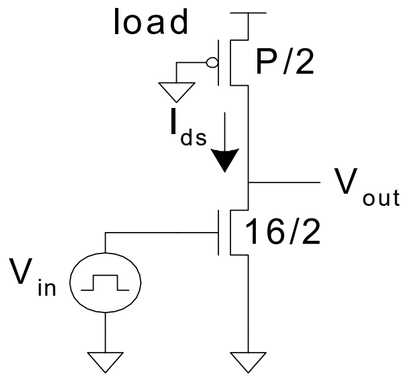
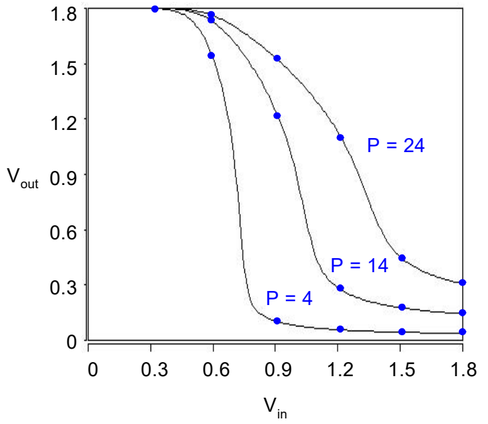
Pseudo-nMOS

In the old days, nMOS processes had no pMOS
- Instead, use pull-up transistor that is always ON

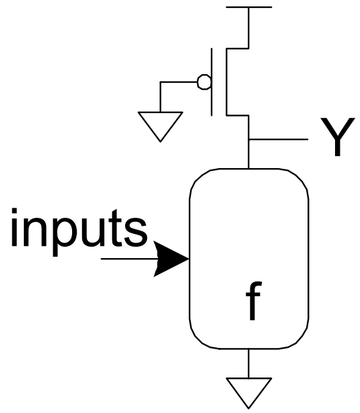
In CMOS, use a pMOS that is always ON
- *Ratio* issue
- Make pMOS about ¼ effective strength of pull down network



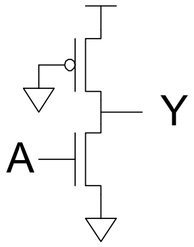


Pseudo-nMOS Gates

- Design for unit current on output to compare with unit inverter.
- pMOS fights nMOS

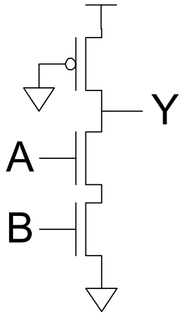


Inverter



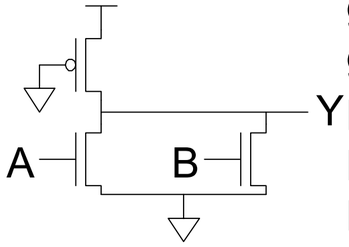
g_u =
g_d =
g_{avg} =
p_u =
p_d =
p_{avg} =

NAND2



g_u =
g_d =
g_{avg} =
p_u =
p_d =
p_{avg} =

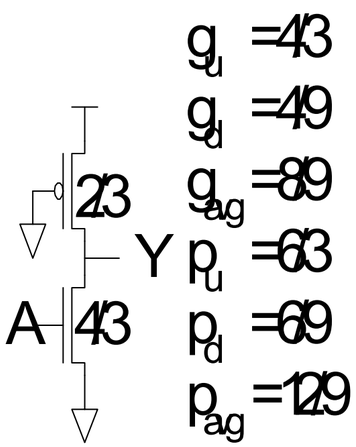
NOR2



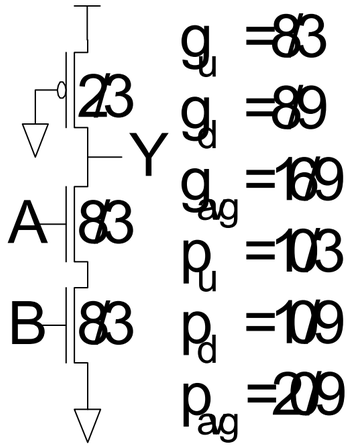
g_u =
g_d =
g_{avg} =
p_u =
p_d =
p_{avg} =

Comparison

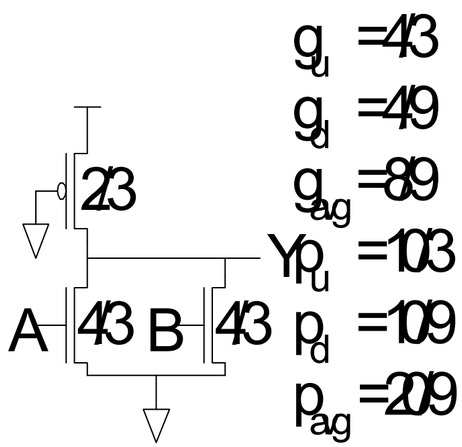
Inverter



NAND2



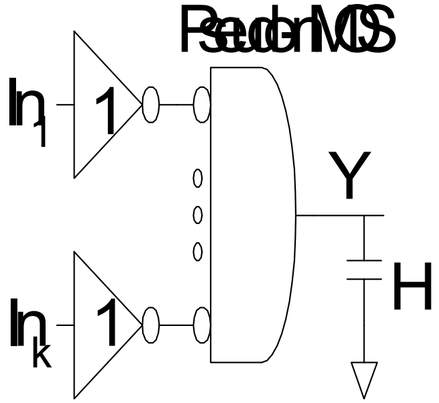
NOR2



Pseudo-nMOS Design

- Ex: Design a k-input AND gate using pseudo-nMOS. Estimate the delay driving a fanout of H

- G = 1 * 8/9 = 8/9
- F = GBH = 8H/9
- P = 1 + (4+8k)/9 = (8k+13)/9
- N = 2
- D = $NF^{1/N} + P = \frac{4\sqrt{2H}}{3} + \frac{8k+13}{9}$



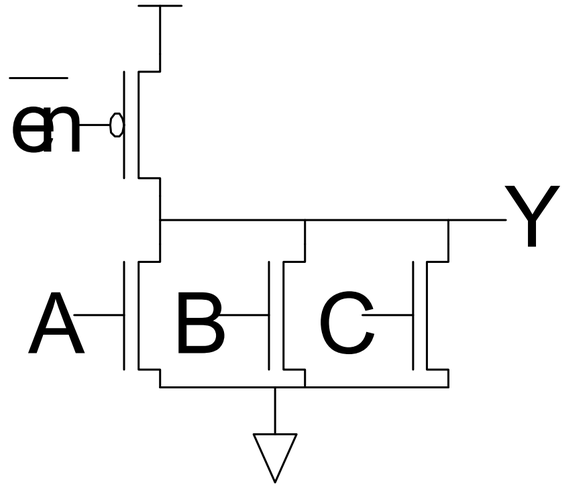
Pseudo-nMOS Power

Pseudo-nMOS draws power whenever Y = 0

- Called static power $P = I \bullet V_{DD}$
- A few mA / gate * 1M gates would be a problem
- This is why nMOS went extinct!

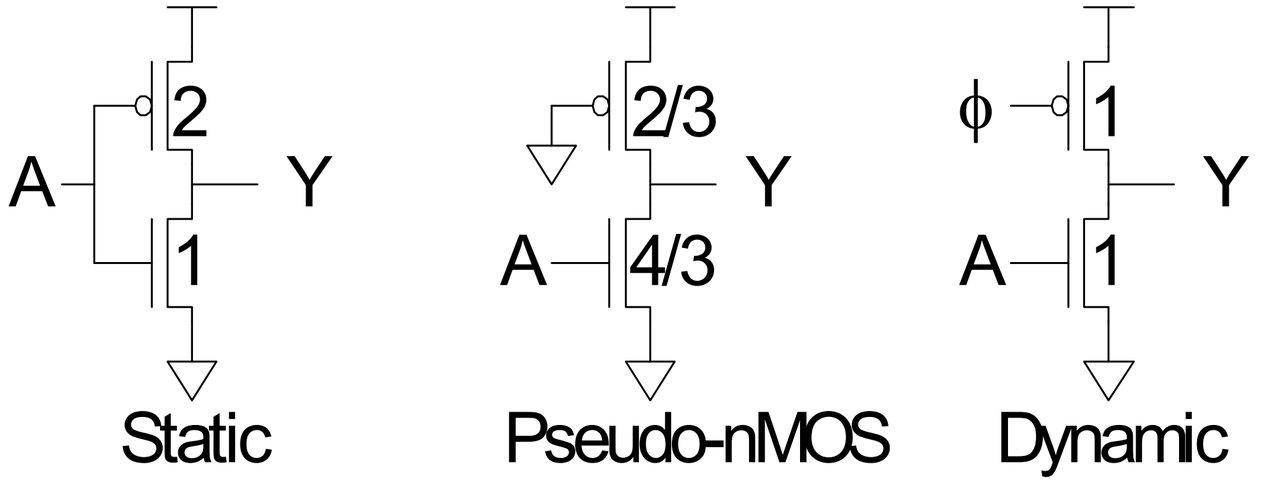
Use pseudo-nMOS sparingly for wide NORs

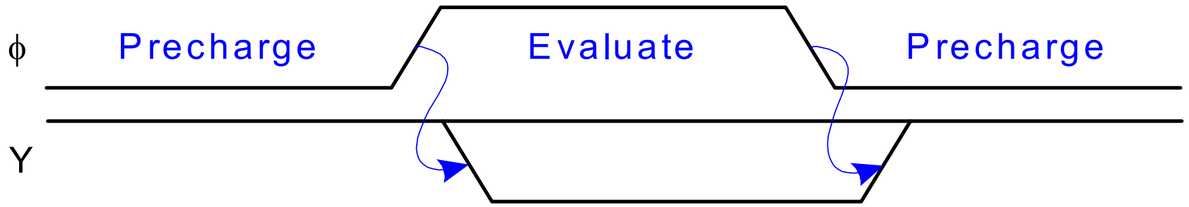
Turn off pMOS when not in use



Dynamic Logic

Dynamic gates uses a clocked pMOS pullup
Two modes: precharge and evaluate

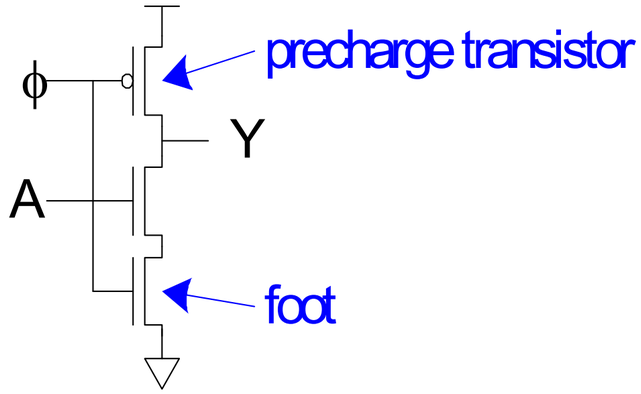


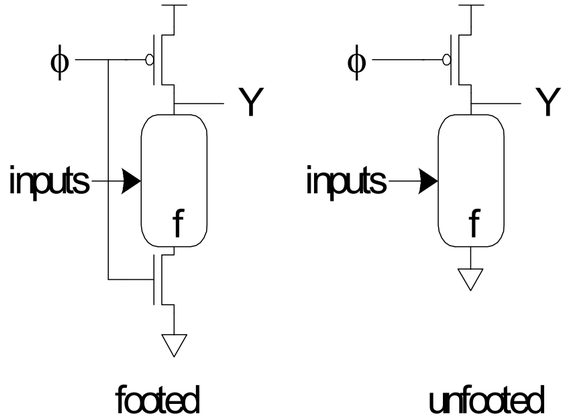


The Foot

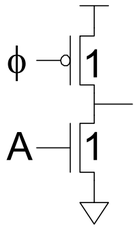
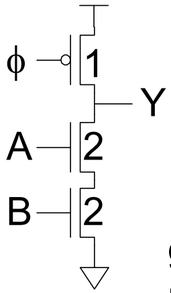
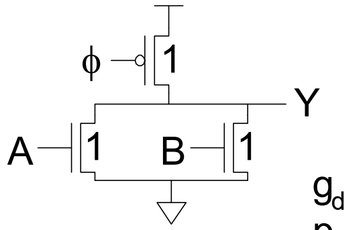
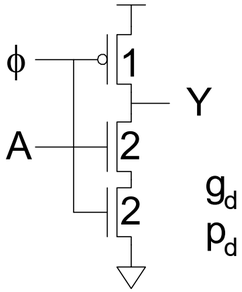
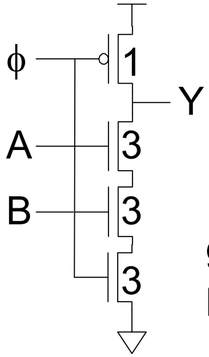
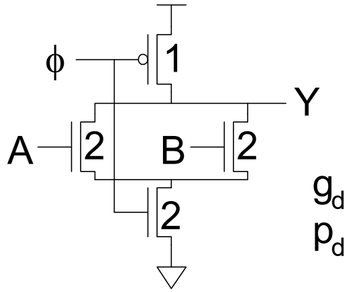
What if pull down network is ON during precharge?

Use series evaluation transistor to prevent fight.





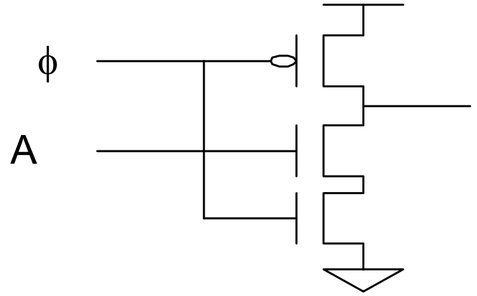
Logical Effort

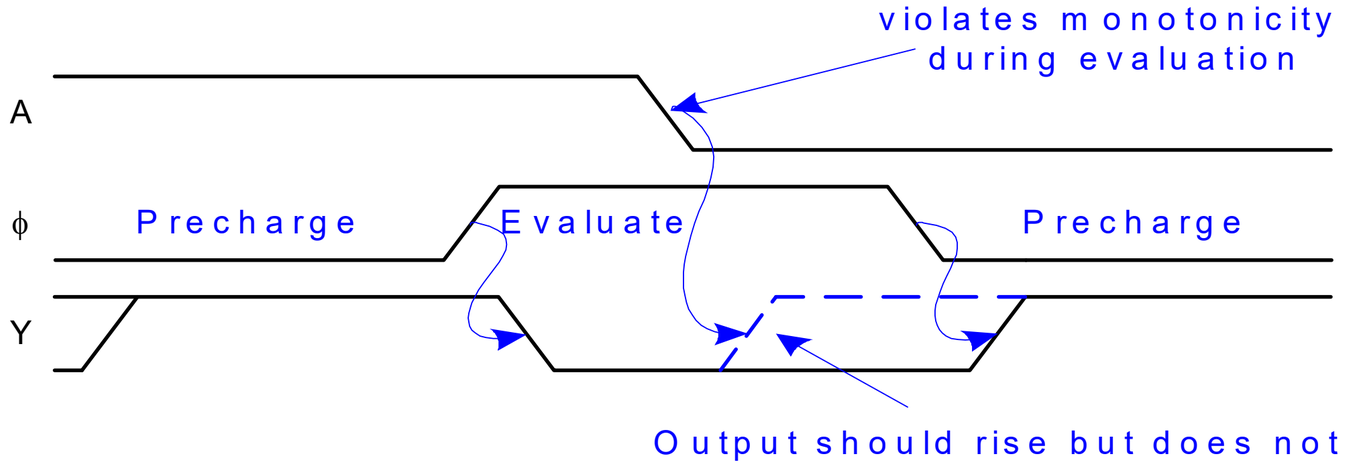
	Inverter	NAND2	NOR2
unfooted	 $g_d = 1/3$ $p_d = 2/3$	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 1/3$ $p_d = 3/3$
footed	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 3/3$ $p_d = 4/3$	 $g_d = 2/3$ $p_d = 5/3$

Monotonicity Problems

Dynamic gates require monotonically rising inputs during evaluation

- 0 -> 0
- 0 -> 1
- 1 -> 1
- But not 1 -> 0

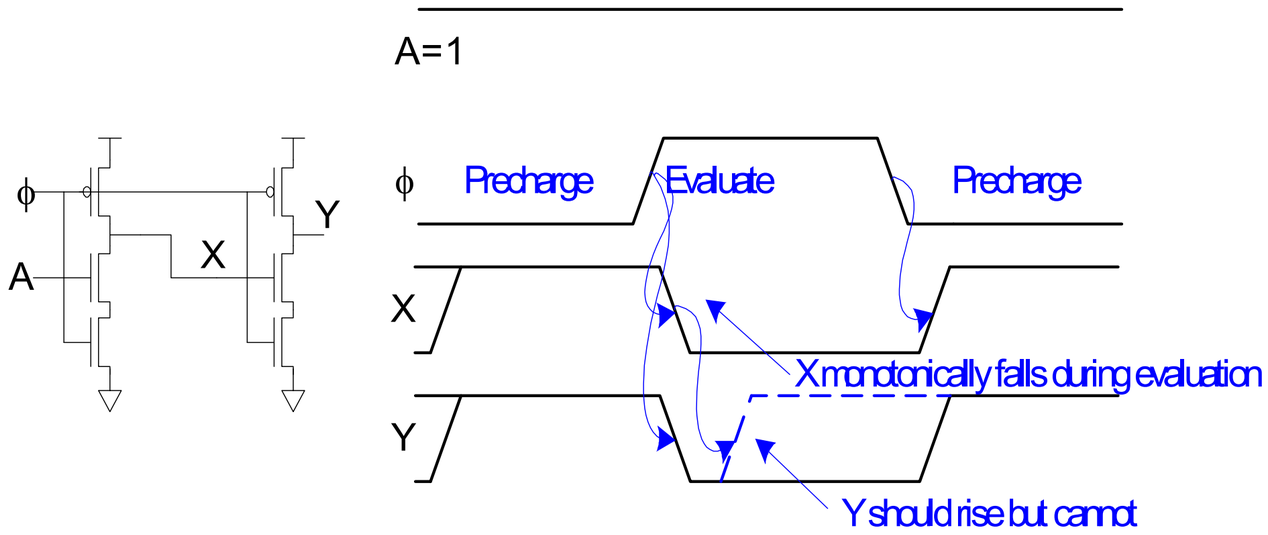




Monotonicity Woes

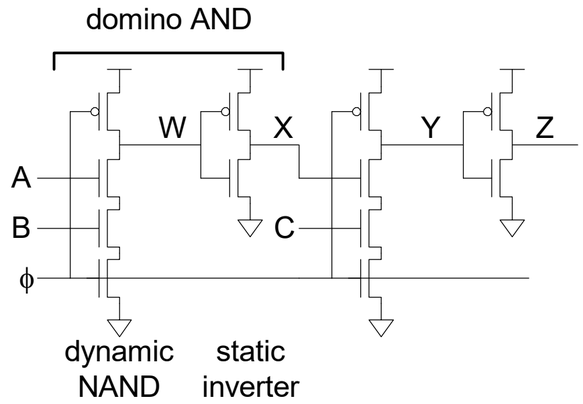
But dynamic gates produce monotonically falling outputs during evaluation

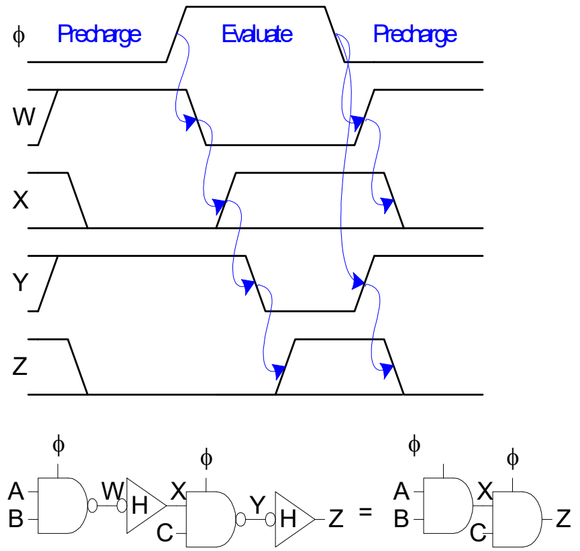
Illegal for one dynamic gate to drive another!



Domino Gates

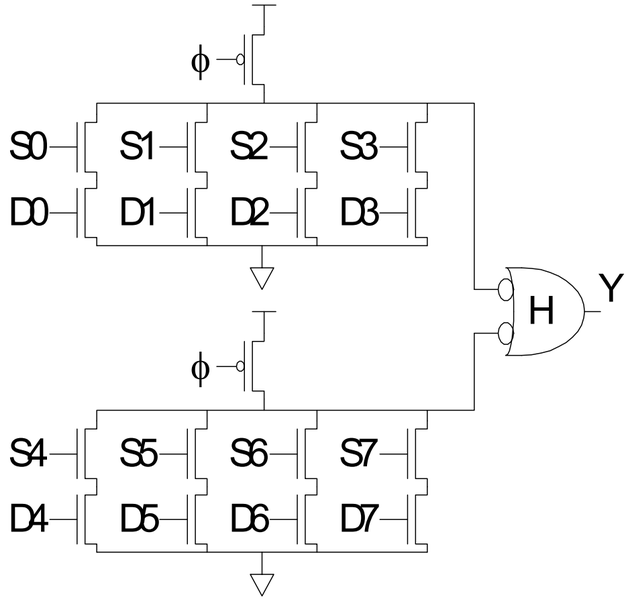
Follow dynamic stage with inverting static gate Dynamic / static pair is called domino gate Produces monotonic outputs





Domino Optimizations

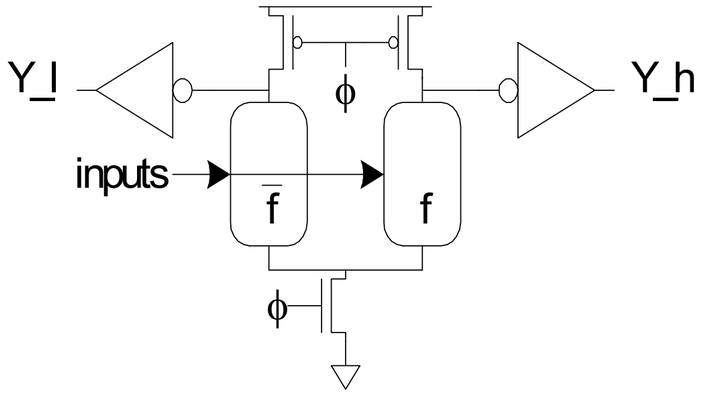
- Each domino gate triggers next one, like a string of dominos toppling over
- Gates evaluate sequentially but precharge in parallel
- Thus evaluation is more critical than precharge
- HI-skewed static stages can perform logic



Dual-Rail Domino

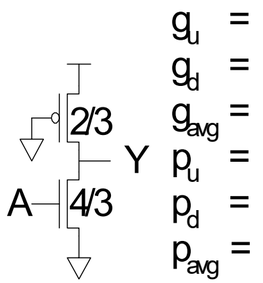
- Domino only performs no inverting functions:
  AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
  Takes true and complementary inputs
  Produces true and complementary outputs

sig_h	sig_l	Meaning
0	0	Precharged
0	1	‘0’
1	0	‘1’
1	1	invalid

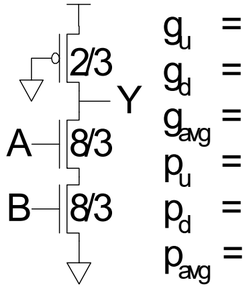


Assessment-Fill up the blanks

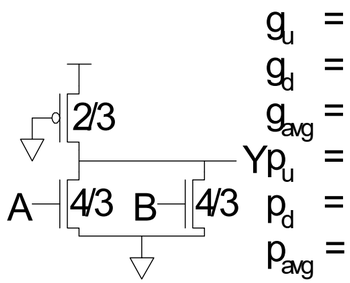
Inverter

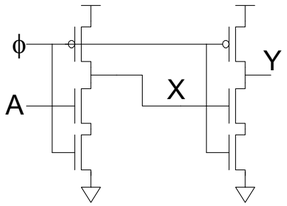


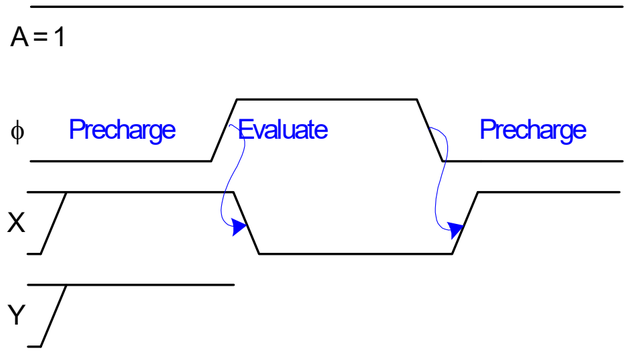
NAND2



NOR2







sig_h	sig_l	Meaning
0	0	
0	1	
1	0	
1	1	

THANK YOU