

SNS COLLEGE OF TECHNOLOGY



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COIMBATORE-641 035, TAMIL NADU

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Name: 23ECT203 LINEAR INTEGRATED CIRCUITS

II YEAR/VI SEMESTER

UNIT I –BASICS OF OPERATIONAL AMPLIFIERS

Topic :DC Characteristics

Introduction to DC Characteristics

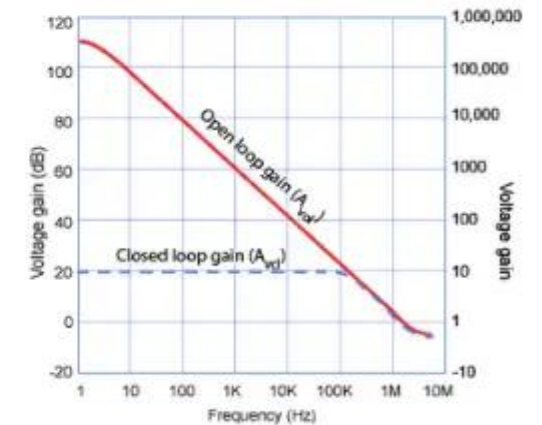
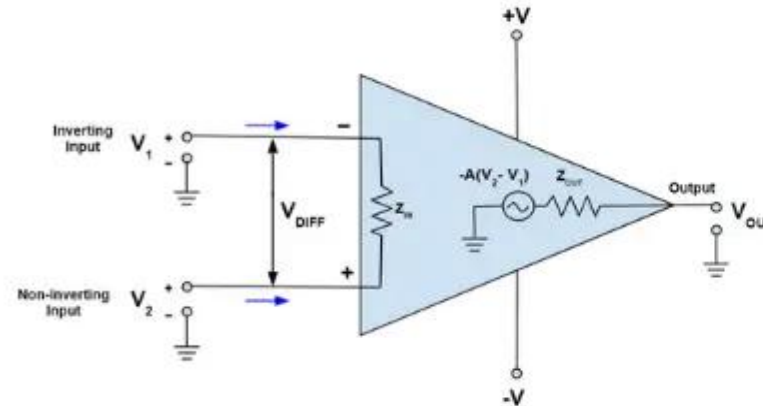
② What are DC Characteristics?

- Parameters describing op-amp behavior with **DC signals**
- Behavior in **quiescent state** (no signal)

! Why are they important?

- Real op-amps are **not ideal**
- DC imperfections cause **output errors**
- Critical for **precision applications**
- Essential for **sensor interfaces** and **instrumentation**

What are the Op Amp Characteristics?



Stage 2: Define

Defining requirements for understanding DC parameters

📋 Learning Goals

- ✓ Define key parameters: **Vos, Ib, Ios**
- ✓ Understand the **physical origin** of each parameter
- ✓ Learn to **model their effect** on a circuit
- ✓ Calculate the resulting **DC output error**



Input Offset Voltage (V_{os})

Voltage needed between inputs to zero output



Input Bias Current (I_b)

Average of currents into the two inputs



Input Offset Current (I_{os})

Difference between the two input currents

Stage 3: Ideate

Brainstorming approaches to analyze DC errors

Approaches

 Analyze **manufacturer datasheets** for typical/max values

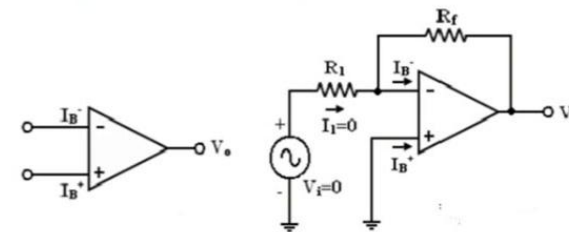
 Use **superposition** to calculate effect of each error source

 Create **simplified DC equivalent** circuit models

 Simulate circuits using **SPICE** to verify calculations

DC Characteristics of op-amp

- Input bias current:**



- I_B^+ & I_B^- are the currents flowing in base of transistors

$$\text{Bias Current } I_B = \frac{I_B^+ + I_B^-}{2}$$

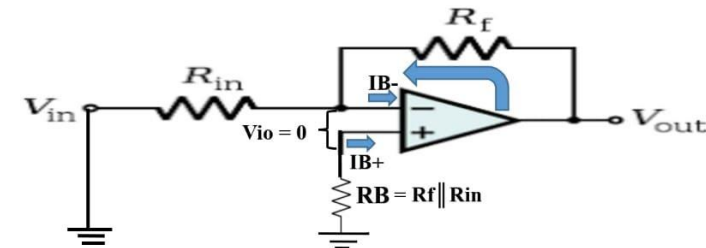
Stage 4: Prototype

Creating a DC error model of an op-amp

🔗 The Model

- 1 Start with an **ideal op-amp symbol**
- 2 Add a **voltage source (V_{os})** in series with one input
- 3 Add **current sources (I_b)** to both inputs
- 4 Model helps **predict the DC error** at the output

OP-Amp Input Bias Current & Input Offset Current

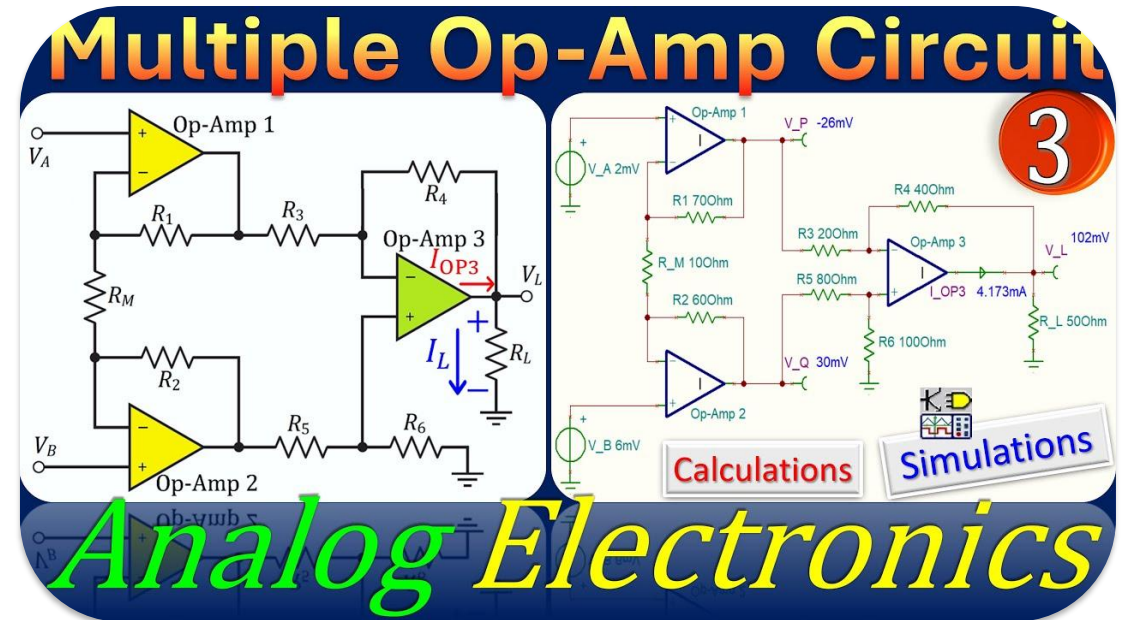


Stage 5: Test

Testing and evaluating DC error calculations





Testing Method

- 1 Choose a **simple circuit** (e.g., inverting amplifier)
- 2 Use the **DC error model** to calculate expected output voltage
- 3 Compare the calculated result with a **SPICE simulation**
- 4 **Analyze discrepancies** and refine the model







Input Bias & Offset Current (I_b & I_{os})

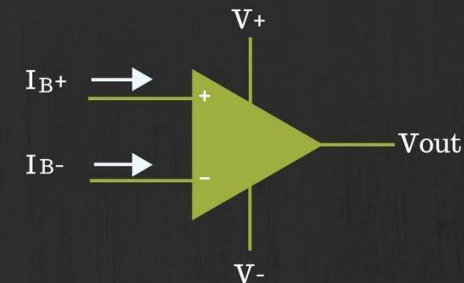
↗ Input Bias Current (I_b)

-  **Definition:** Average of currents into the two inputs
-  **Formula:** $I_b = (I_{b+} + I_{b-}) / 2$
-  **Cause:** Base bias current of differential input transistors
-  **Typical Values:** Nanoamps (nA) range

↔ Input Offset Current (I_{os})

-  **Definition:** Difference between the two input currents
-  **Formula:** $I_{os} = |I_{b+} - I_{b-}|$
-  **Cause:** Mismatch in input transistor betas (β)
-  **Typical Values:** 10-20% of I_b

Input Bias Current and Input Offset Current



Input Offset Voltage (V_{os})

⚡ Definition

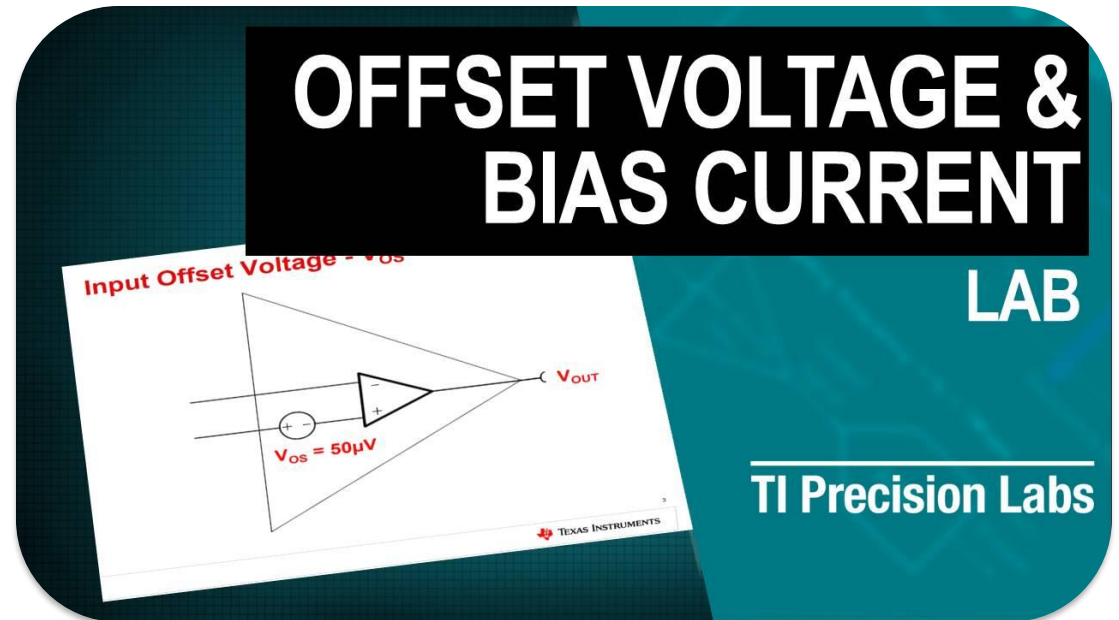
📄 DC voltage that must be applied between inputs to force output to **zero volts**

🔧 Cause

- ➔ Mismatches in input stage transistors:
 - ▶ Base-emitter voltage (V_{be}) differences
 - ▶ Collector resistance (R_c) differences

⚡ Effect & Values

- 📈 Acts like a **small DC source** in series with input
- ⚠️ Causes **output error** proportional to circuit gain
- 🕒 Typical values: **1-5 mV** for 741 op-amp



Output DC Errors & Minimization

⚠ Total Output Error

+ Sum of errors caused by **Vos**, **Ib**, and **Ios**

$$\Sigma V_{\text{error_out}} = (1 + R_f/R_1) \times V_{\text{os}} + R_f \times I_b + R_f \times I_{\text{os}}$$

⚙ Minimizing Ib Error

⊕ Add **compensating resistor** (R_{comp}) to non-inverting terminal

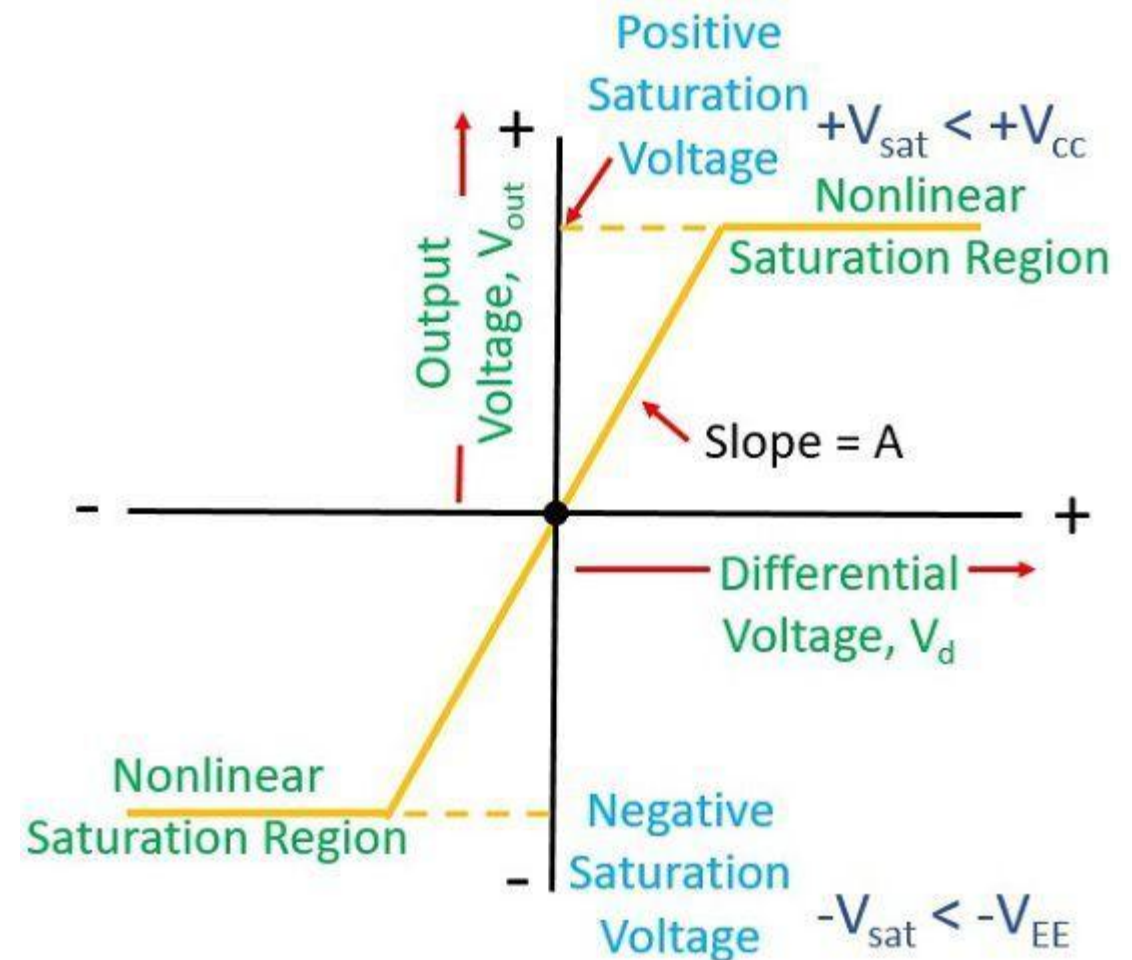
$$\Sigma R_{\text{comp}} = R_1 \parallel R_f \text{ (for inverting amp)}$$

⚖ Makes resistance seen by both inputs **equal**

⋯ Other Parameters

🛡 **CMRR**: Rejects common-mode DC

🔌 **PSRR**: Rejects supply ripple



Activity: THINK-PAIR-SHARE



THINK (2 min)

An inverting amplifier has a gain of -10 and a **Vos** of 2mV. What is the output DC error due to Vos alone?



PAIR (3 min)

Discuss your calculation and method with a partner



SHARE (5 min)

Be ready to share your answer and the formula you used



Individual Thinking

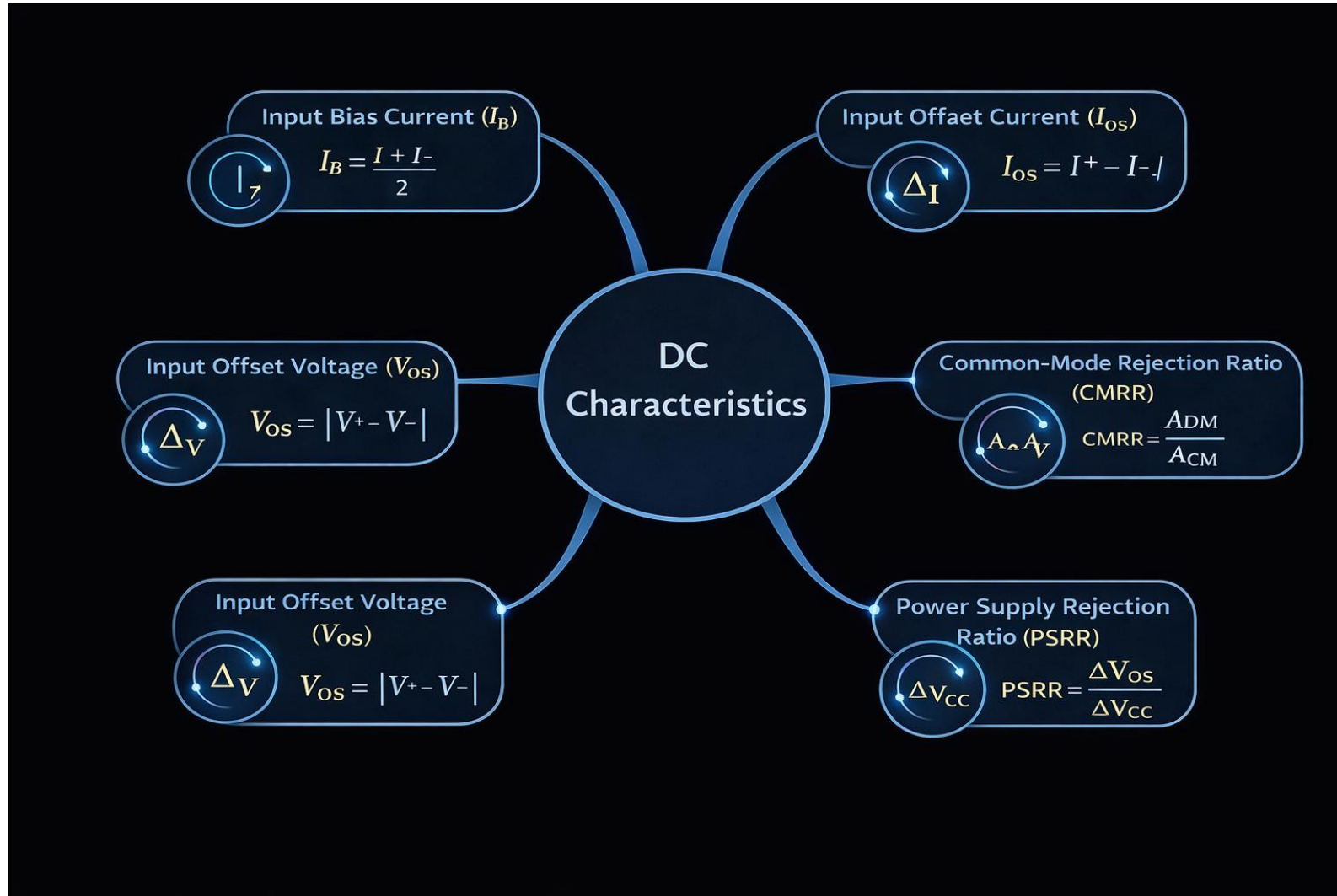


Partner Discussion



Group Sharing

Summary: Mind Map



Exam-Oriented Questions

1 Define **Input Offset Current** and state its typical value for a 741 op-amp.

2 Draw the **DC error model** of an op-amp including V_{os} and I_b .

3 Why is a resistor connected to the **non-inverting terminal** of an op-amp in a practical inverting amplifier?

4 List two causes for **input offset voltage**.



References

Textbooks



D.Roy Choudhry, Shail Jain, "**Linear Integrated Circuits**", New Age International, 5th edition, 2018. (Unit I, Section 1.4)



Sergio Franco, "**Design with Operational Amplifiers and Analog Integrated Circuits**", 4th Edition, Tata Mc Graw-Hill, 2014. (Chapter 2)

Online Resource



Texas Instruments, "**Op-amp Basics: Introduction to the Operational Amplifier**", [Link to TI E2E or technical document]



Textbooks



Online Resources

THANK YOU