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COIMBATORE-641 035, TAMIL NADU

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Name: 23ECT203 LINEAR INTEGRATED CIRCUITS

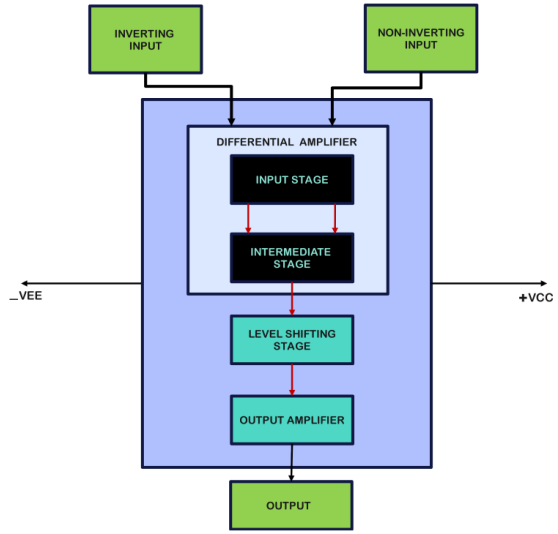
II YEAR/VI SEMESTER

UNIT I –BASICS OF OPERATIONAL AMPLIFIERS

Topic : General operational amplifier stages

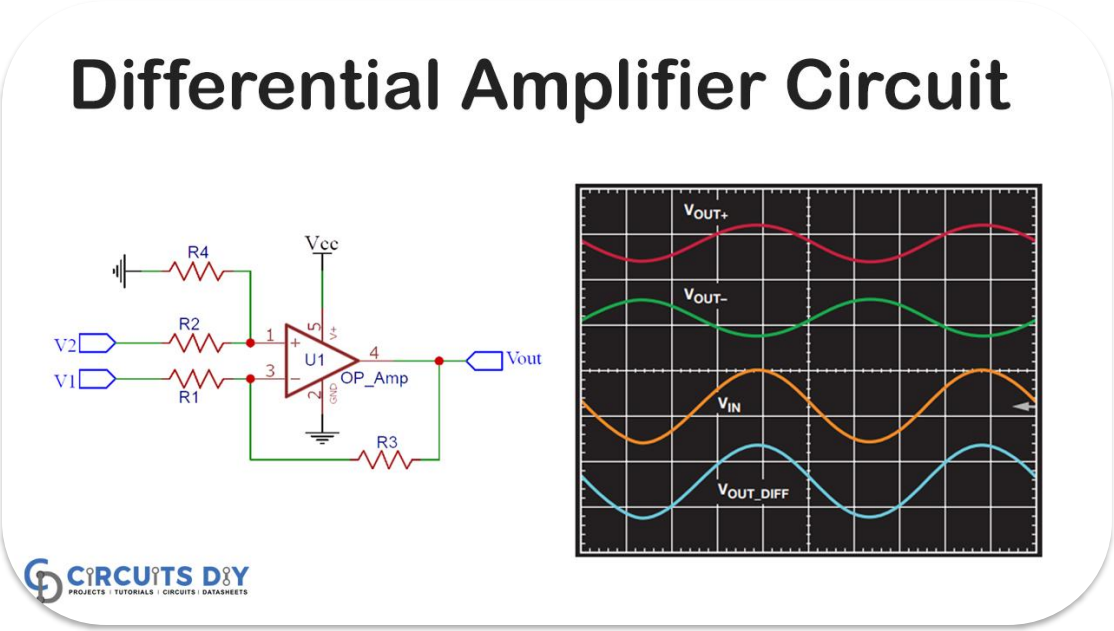
Introduction to Op-Amp Stages

- **Operational amplifiers** consist of cascaded stages that collectively determine performance
- **Three main stages** work together to provide high gain, input impedance, and low output impedance
- **Input stage** provides differential amplification with high input impedance
- **Intermediate stage** provides additional voltage gain and frequency compensation
- **Output stage** provides low output impedance and current drive capability



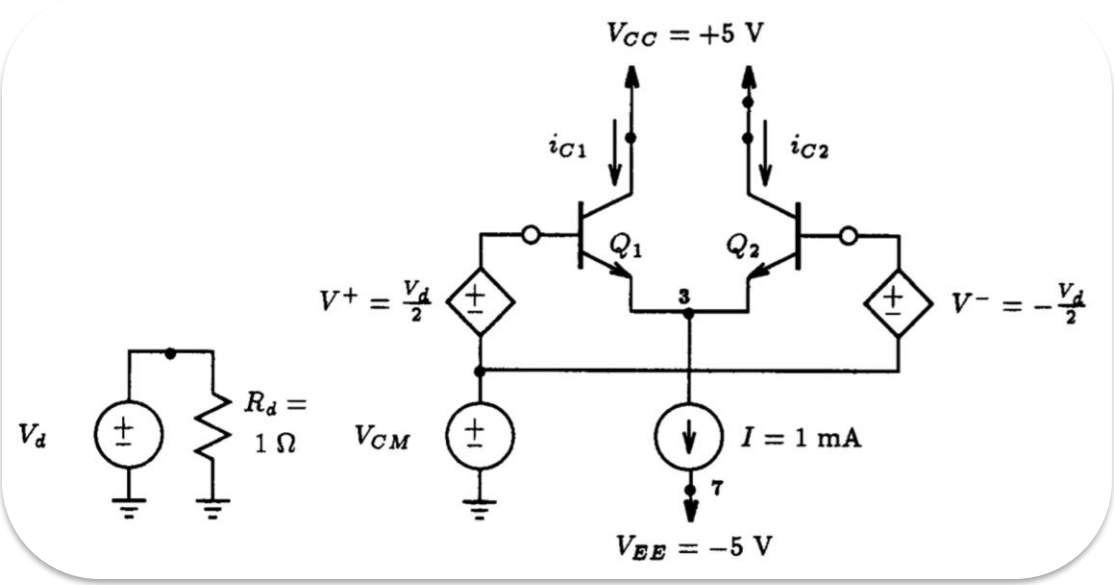
Empathize

- **Signal Distortion** - Poor stage design causes amplitude and phase distortion
- **Bandwidth Limitations** - Cascaded stages reduce overall frequency response
- **Power Consumption** - Each stage contributes to total power draw
- **Noise Issues** - Input stage noise amplified by subsequent stages
- **Temperature Effects** - Stage performance varies with temperature
- **Manufacturing Variations** - Component tolerances affect stage matching



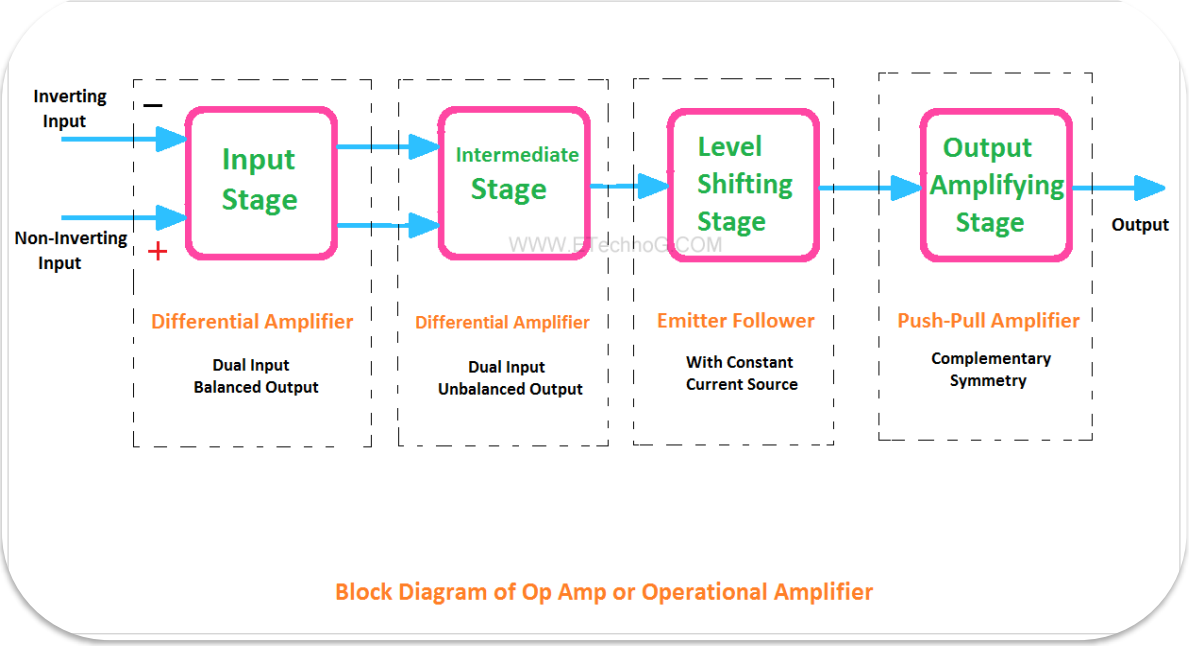
Define

- **Input Stage** - High input impedance (>1MΩ), high CMRR (>80dB), low offset voltage
- **Intermediate Stage** - High voltage gain (>10,000), frequency compensation, phase margin
- **Output Stage** - Low output impedance (<100Ω), high slew rate, current drive capability
- **Bandwidth** - Unity gain bandwidth must exceed application requirements
- **Power Consumption** - Balance between performance and power efficiency
- **Stability** - Ensure proper phase margin to prevent oscillation



Ideate

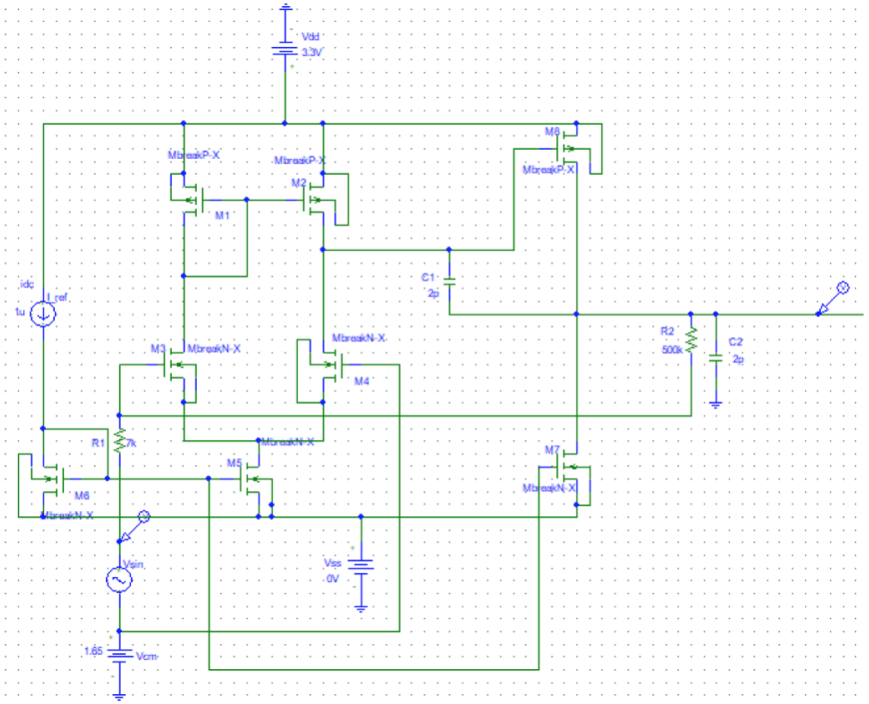
- **Input Stage Options** - Differential pairs, Darlington, cascode configurations
- **Intermediate Stage Options** - Common-emitter, Darlington, current mirror loading
- **Output Stage Options** - Class A, Class AB, push-pull configurations
- **Component Selection** - Matching transistors, precision resistors, temperature-stable devices
- **Compensation Techniques** - Miller, pole-zero, lead-lag networks
- **Innovative Approaches** - Chopper stabilization, auto-zeroing, current-mode design



Block Diagram of Op Amp or Operational Amplifier

Prototype

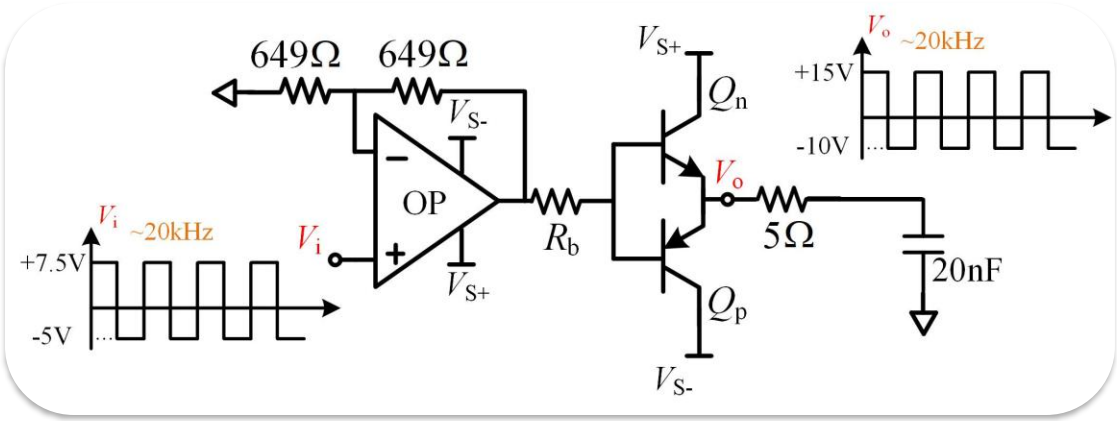
- **Simulation Tools** - SPICE, Multisim, Proteus for circuit analysis
- **Breadboarding** - Modular testing of individual stages before integration
- **PCB Prototyping** - Custom boards for high-frequency performance
- **Testing Methodologies** - Frequency response, transient analysis, noise measurement
- **Component Matching** - Precision selection for differential pairs
- **Iterative Refinement** - Adjust component values based on test results



< PSPICE Schematics >

Test

- **Frequency Response** - Measure gain vs. frequency to verify bandwidth
- **Transient Response** - Test slew rate and settling time with step input
- **Input Characteristics** - Measure input impedance and bias current
- **Output Characteristics** - Test output impedance and current drive capability
- **CMRR & PSRR** - Verify rejection of common-mode and power supply noise
- **Temperature Testing** - Verify performance across operating temperature range



Activity

THINK (2 minutes)

Identify key challenges in designing each op-amp stage. Consider trade-offs between performance parameters.

PAIR (2 minutes)

Discuss your findings with a partner. Compare your identified challenges and propose solutions.

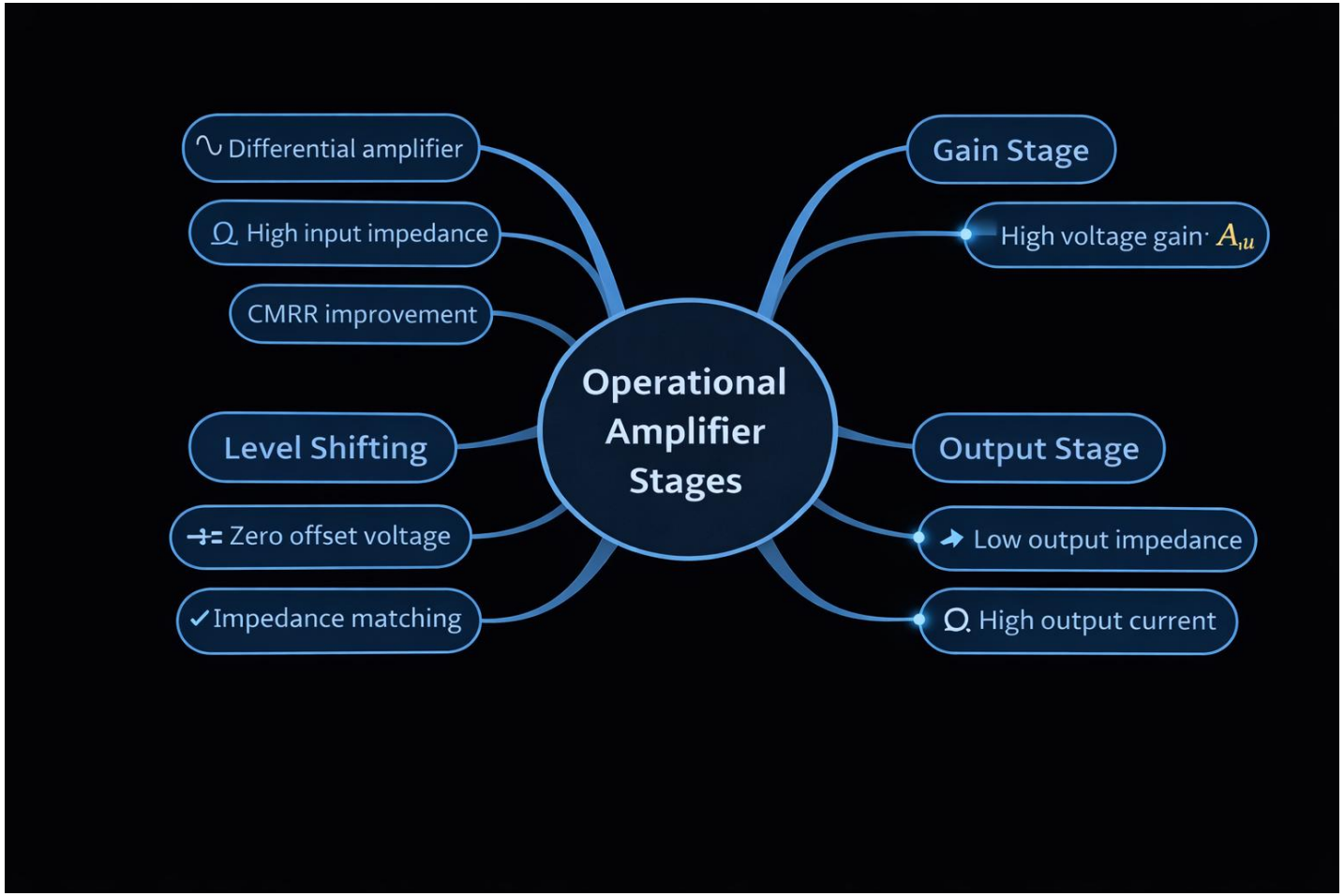
SHARE (1 minute)

Share your group's most significant challenge and proposed solution with the class.

Expected Outcomes

- Identify stage-specific challenges
- Understand design trade-offs
- Develop problem-solving skills
- Apply theoretical knowledge

Summary: Mind Map



Assessment

Multiple Choice Questions

1. Which stage provides the highest voltage gain in an op-amp?
2. What is the primary function of the output stage?
3. Which configuration is typically used in the input stage?

Short Answer Questions

4. Explain the purpose of frequency compensation in the intermediate stage.
5. Describe the advantages of a Class AB output stage.
6. How does a differential input stage improve CMRR?

References

Textbooks

- **D. Roy Choudhry, Shail Jain**, "Linear Integrated Circuits", New Age International Pvt. Ltd., Fifth edition 2018.
- **Sergio Franco**, "Design with Operational Amplifiers and Analog Integrated Circuits", Fourth Edition, Tata Mc Graw-Hill, 2014.
- **Ramakant A. Gayakwad**, "OP-AMP and Linear ICs", 4th Edition, Prentice Hall/Pearson Education, 2001.

Online Resources

- **NPTEL** - Linear Integrated Circuits Course (nptel.ac.in)
- **Texas Instruments** - Op-Amp Design Handbook (ti.com)
- **Analog Devices** - Op-Amp Applications Handbook (analog.com)

Thank You