SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai
Accredited by NAAC-UGC with 'A++' Grade (Cycle III) &
Accredited by NBA (B.E - CSE, EEE, ECE, Mech & B.Tech.IT)
COIMBATORE-641 035, TAMIL NADU

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Course Name: 23ECT203 LINEAR INTEGRATED CIRCUITS

II YEAR/VI SEMESTER

UNIT I –BASICS OF OPERATIONAL AMPLIFIERS

Topic :Input Bias Current

Introduction

ⓘ What is Input Bias Current?

Average current flowing into both input terminals of an op-amp

! Why is it Important?

- Creates DC errors in precision circuits
- Affects output voltage through resistive networks
- Limits performance in high-impedance applications

Impact on Circuit Performance

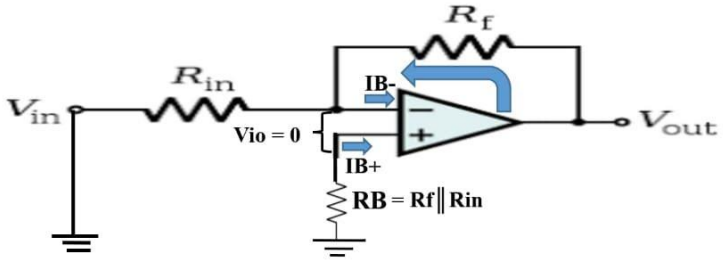
- Causes output voltage offset
- Degrades accuracy in measurement systems
- Particularly critical in low-frequency applications

OP-Amp

Input Bias Current

&

Input Offset Current

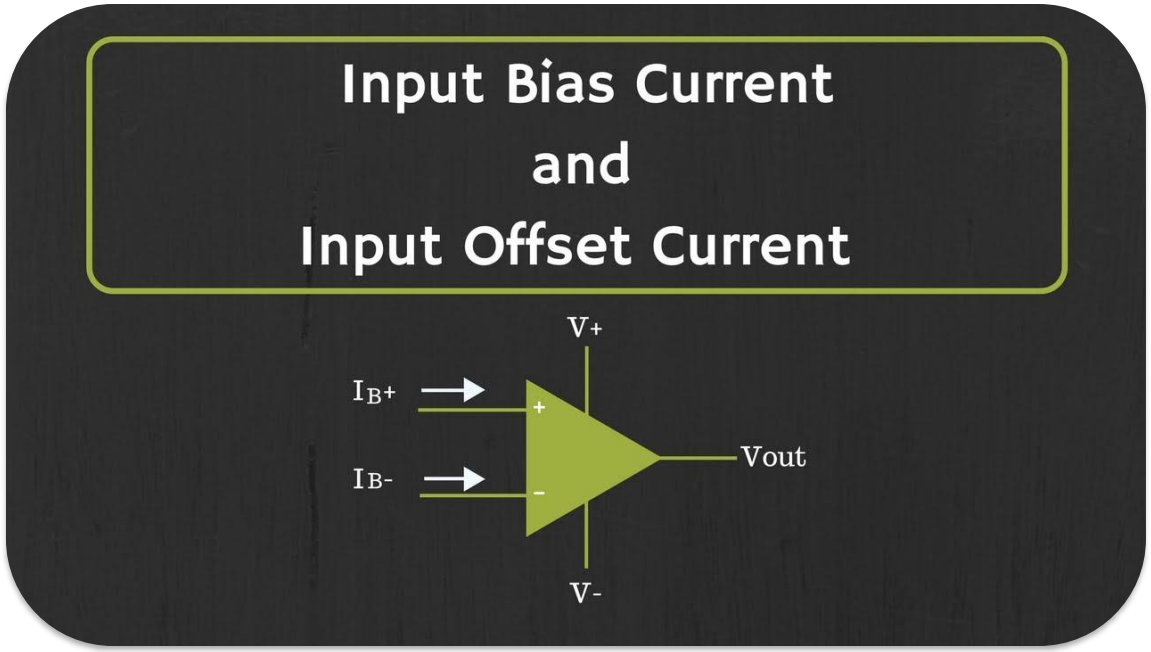


Stage 1: Empathize

Understanding Challenges

Student Challenges

- Visualizing nanoampere-level currents
- Connecting datasheet values to circuit behavior
- Understanding impact on high-impedance circuits
- Distinguishing between bias current and offset current



Stage 2: Define

Learning Goals

Key Objectives

- Define key parameters: Ib and Ios
- Understand physical origin of bias currents
- Model their effect on circuit performance
- Calculate resulting DC output errors

Parameters of OP-AMP

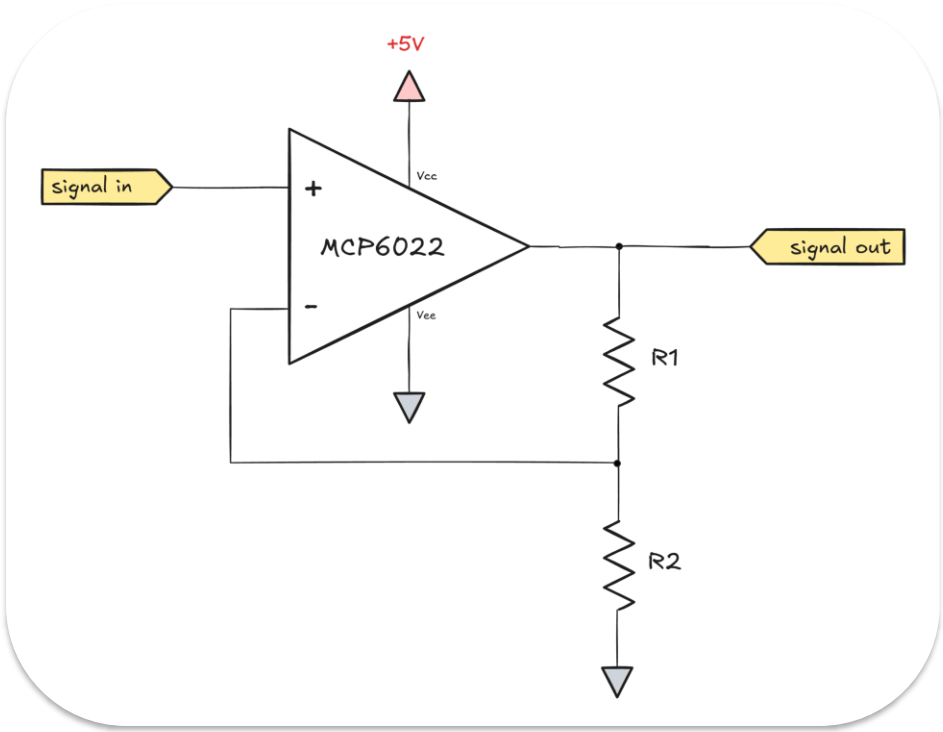
- Input offset voltage
- Input offset current
- Input BIAS current
- Large signal voltage gain
- Output voltage swing
- Differential input resistance Ri
- Input capacitance Ci
- Common mode rejection ratio
- Supply voltage rejection ratio
- Slew rate
- Gain bandwidth product

Stage 3: Ideate

Brainstorming Approaches

Analysis Methods

- Analyze manufacturer datasheets for typical/max values
- Use superposition to calculate effect of each error source
- Create simplified DC equivalent circuit models
- Simulate circuits using SPICE to verify calculations

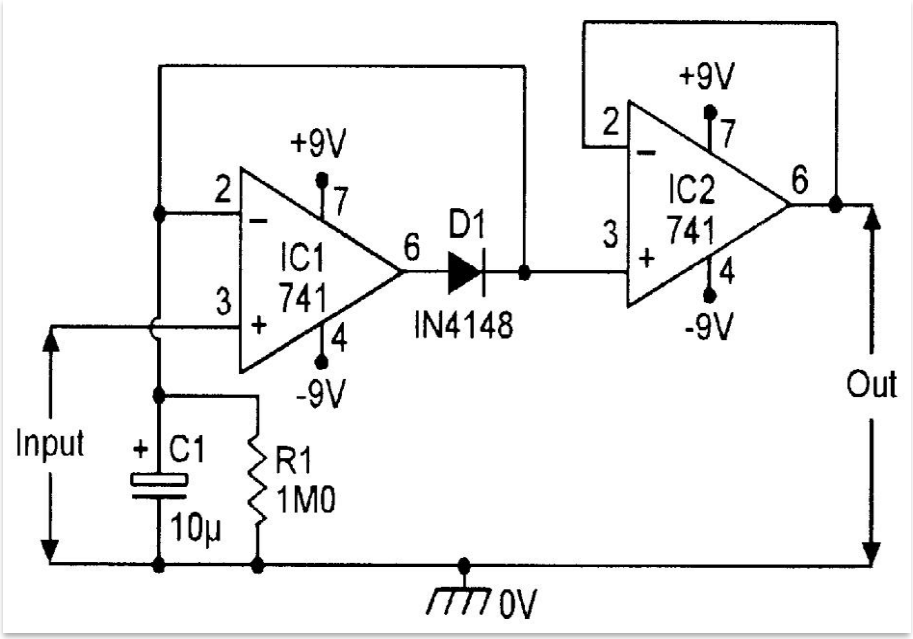


Stage 4: Prototype

Input Bias Current Model

Model Construction

- Start with **ideal op-amp** symbol
- Add **current sources** (Ib) to both inputs
- Include **offset current** (Ios) if needed
- Predicts **DC error** at output

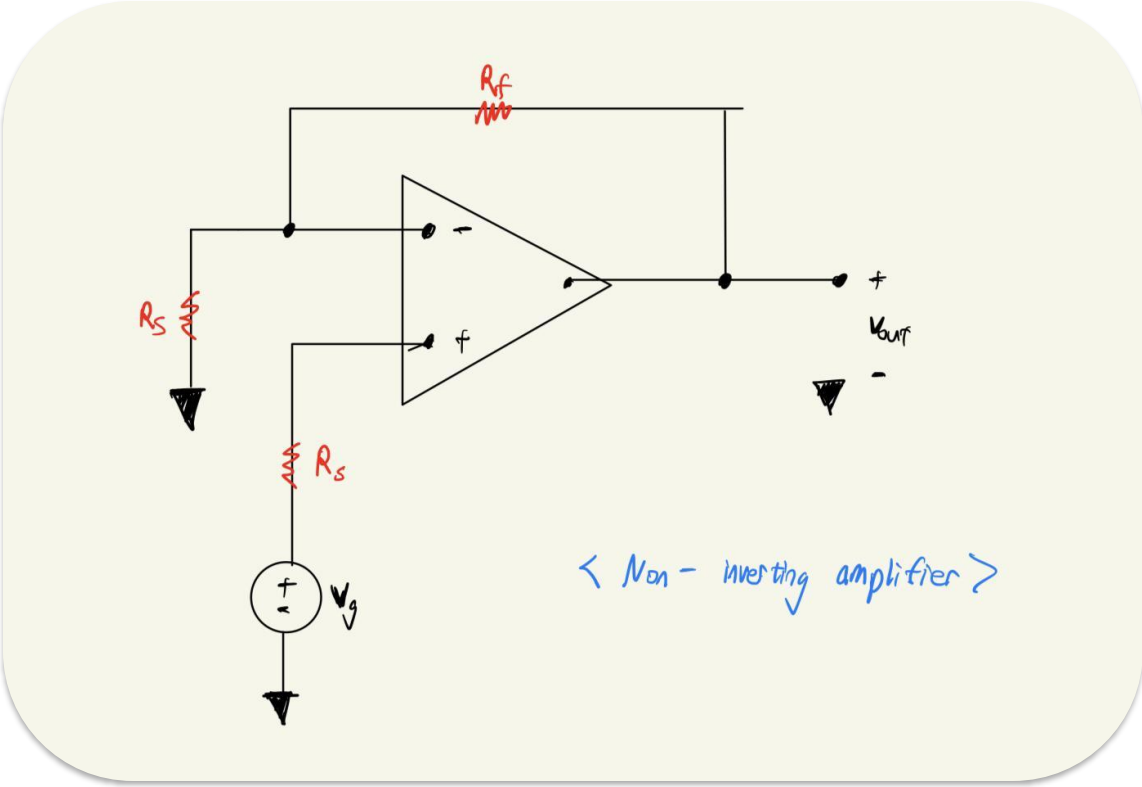


Stage 5: Test

Testing Methods

Validation Process

- Choose **simple circuit** (inverting amplifier)
- Use **bias current model** to calculate output
- Compare with **SPICE simulation** results
- Analyze **discrepancies** and refine model

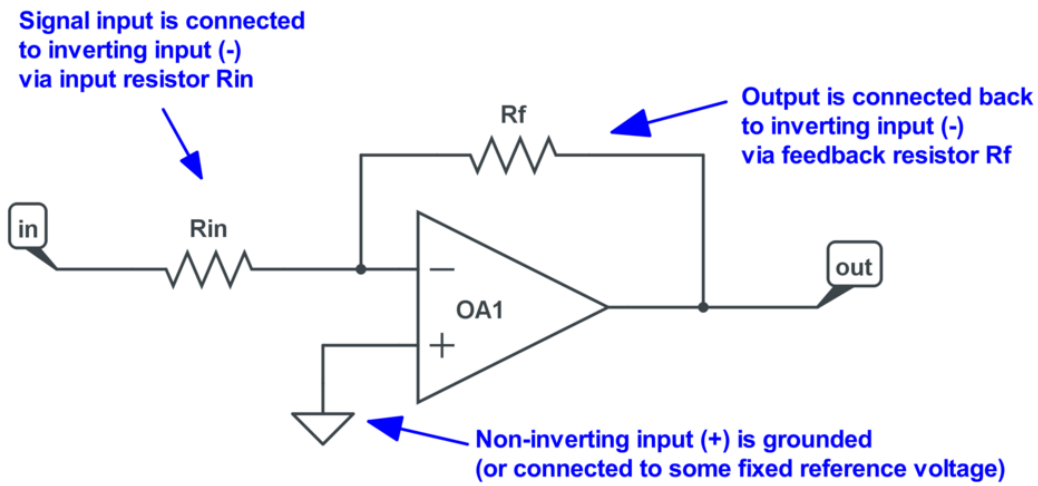


Input Bias Current

Definition

$$Ib = (Ib+ + Ib-) / 2$$

- Average of currents into **both input terminals**
- Cause: **Base bias current** of differential input transistors
- Typical values: **nanoampere range** (10-100 nA)
- Creates **DC offset** in output voltage



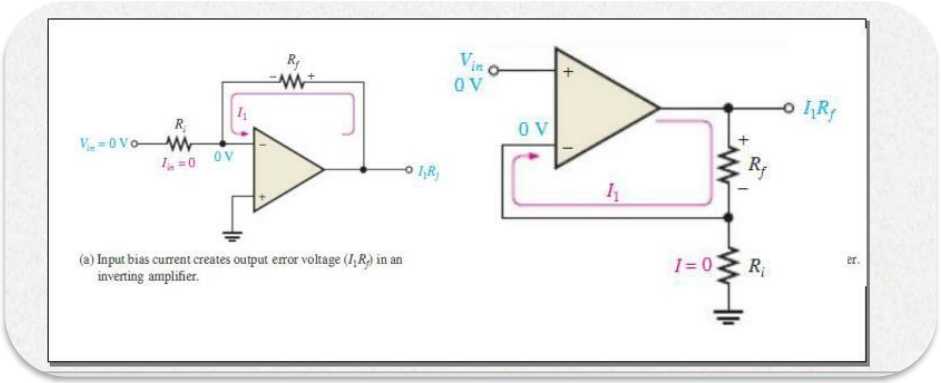
OP-AMP INVERTING AMPLIFIER

Input Bias & Offset Current

Input Offset Current (Ios)

Ios = |Ib+ - Ib-|

- Difference between the **two input currents**
- Cause: **Mismatch** in input transistor betas (β)
- Typical values: **10-20% of Ib**
- Creates **additional DC error** in output voltage



(a) Input bias current creates output error voltage (I_1R_f) in an inverting amplifier.

Activity: THINK-PAIR-SHARE

Instructions

1 **THINK (2 min)**

An inverting amplifier has R1 = 10kΩ and Rf = 100kΩ. If the op-amp has an input bias current of 80nA, what is the output DC error due to Ib alone?

2 **PAIR (3 min)**

Discuss your calculation and method with a partner.

3 **SHARE (5 min)**

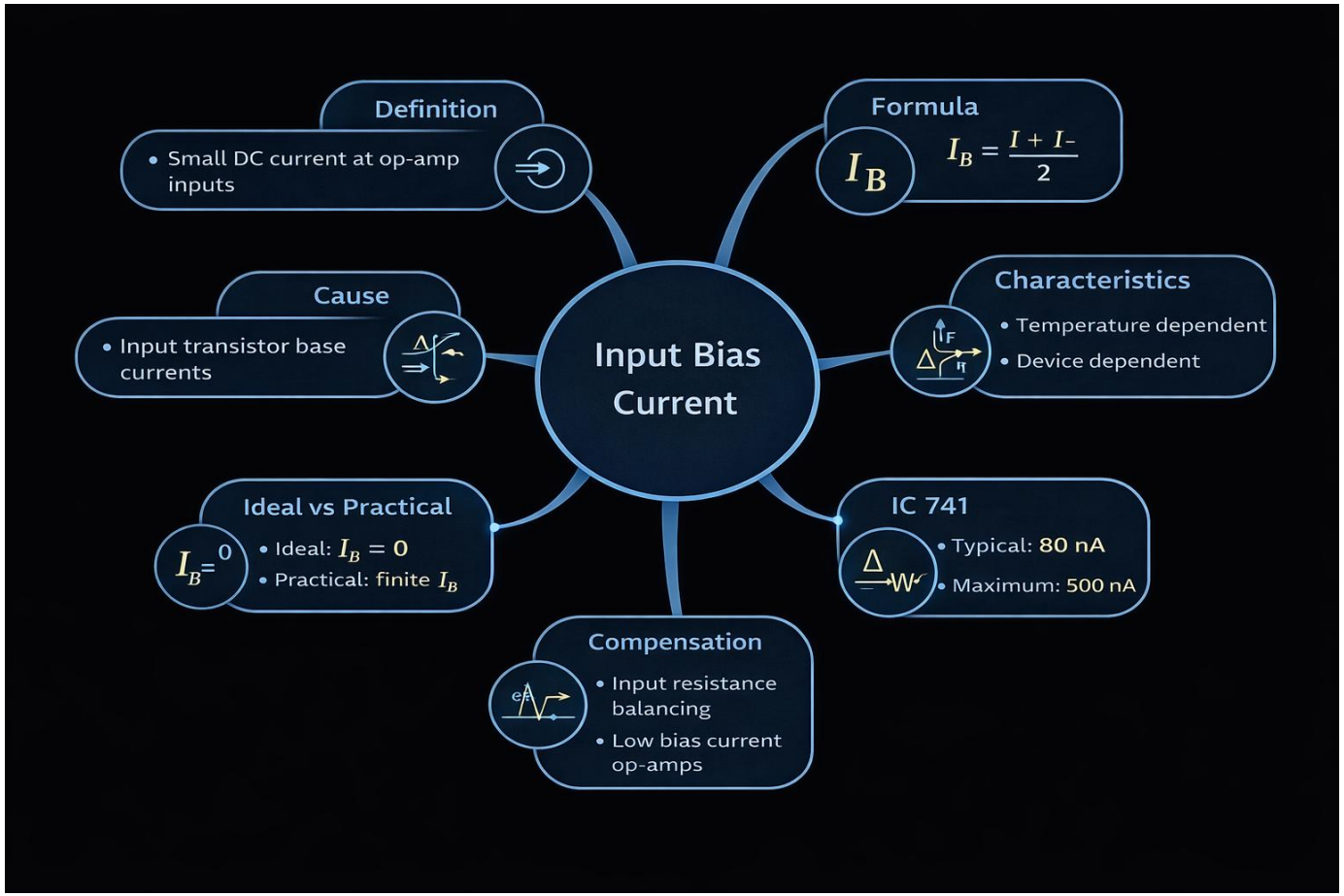
Be ready to share your answer and the formula you used.

Expected Outcome

$V_{error\_out} = I_b \times R_{comp} = I_b \times (R_1 \parallel R_f)$

$= 80nA \times (10k\Omega \parallel 100k\Omega) = 80nA \times 9.09k\Omega = \mathbf{727\mu V}$

Summary:Mind Map



Assessment

Exam-Oriented Questions

1 Define **Input Bias Current** and state its typical value for a 741 op-amp.

2 Draw the input bias current model of an op-amp including **Ib** and **Ios**.

3 Why is a resistor connected to the non-inverting terminal of an op-amp in a practical inverting amplifier?

4 List two causes for input offset current.

References

Textbooks

- D.Roy Choudhry, Shail Jain, **"Linear Integrated Circuits"**, New Age International, 5th edition, 2018. (Unit I, Section 1.4)

- Sergio Franco, **"Design with Operational Amplifiers and Analog Integrated Circuits"**, 4th Edition, Tata Mc Graw-Hill, 2014. (Chapter 2)

Online Resource

- Texas Instruments, **"Op-amp Basics: Introduction to the Operational Amplifier"**, [Link to TI E2E or technical document]

Thank You!